MODEL NO. F649-40

SERIAL NO. 320700957

PHASE ENCODED FORMATTER MODEL F6X9

PERTEC
PERIPHERAL EQUIPMENT

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OPERATING AND SERVICE MANUAL NO. 101399

FOREWORD

This manual provides operating and service instructions for Phase Encoded Formatters Model F6X9, manufactured by PERTEC Peripheral Equipment, Chatsworth, California.

The content includes a detailed description, specifications, and installation instructions. Also included is the definition of interface functions with regard to timing, levels, and interrelationships.

Revised December 1971

SERVICE AND WARRANTY

This PERTEC product has been rigorously checked out by capable quality control personnel. The design has been engineered with a precise simplicity which should assure a new level of reliability. Ease of maintenance has been taken into consideration during the design phase with the result that all components (other than mechanical components) have been selected wherever possible from manufacturer s "off the shelf" stock. Should a component fail, it may be readily replaced from PERTEC or your local supplier. The unit has been designed for "plug-in" replacement of circuit boards or major components which will ensure a minimum of equipment down time.

PERTEC warrants products of its manufacture to be free from defects in design, workmanship, and material under normal and proper use and service for a period of twelve (12) months after the date of shipment. PERTEC agrees to repair or replace at the place of manufacture, without charge, all parts of said products which are returned, for inspection, to its factory within the applicable warranty period, provided such inspection discloses that the defects are as above specified and provided a l s o that the equipment has not been altered or repaired other than with authorization from PERTEC and by its approved procedures, subjected to misuse, improper maintenance, negligence, or accident, damaged by excessive current or otherwise, or had its serial number or any part thereof altered, defaced or re - moved. This warranty is in lieu of all other warranties, expressed or implied, including those of merchantability or fitness for purpose.

Please read the instruction manual thoroughly as to operation, maintenance, and component reference list. Should you require additional assistance in servicing this equipment, please contact the following regional service centers. A trained service representative will be pleased to assist you.

SALES AND SERVICE REPRESENTATIVES

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*Chicago, Ill.	(312) 696-2460	Nieuwkoop, Holand	2614
*Waltham, Mass.	(617) 891-0720	Haifa, Israel	(04) 68234
Sydney, Australia	69-0444	Milano, Italy	5462641
Brussels, Belgium	2-480586	Tokyo, Japan	210-4602
Naerum, Denmark	(01) 804200	Oslo, Norway	550750
*London, England	Reading 582-115	Johannesburg, So. Africa	42-1939
Helsinki, Finland	460844	Madrid, Spain	2560265
Clamart, France	6445530	Solna, Sweden	820410

*Indicates PERTEC-operated service center

PROPRIETARY NOTICE

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SECTION I

GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

This section provides a physical description, functional description, and specifications for the Phase Encoded Formatters Models F609, F619, F629, F649, manufactured by PERTEC Peripheral Equipment, Chatsworth, California.

1.2 PURPOSE OF EQUIPMENT

The PE formatter enables the generation and reading of Phase Encoded ANSI and IBM compatible magnetic tapes when used in conjunction with PERTEC Models 6640, 6660, 7640, and 7620 Magnetic Tape Transports. Data encoding, decoding, deskewing, error correction, and tape motion control are provided by the formatter.

Individual selection and operation with up to four "daisy-chained" PERTEC transports is provided. Normally, all transports attached to a formatter must be of the same speed, but can be a mixture of Read/Write (single stack head) or Read after Write (dual stack head).

A dual speed option is also available which allows the formatter to operate with transports having two different tape speeds. This option should be specified at the time of ordering.

The formatter is capable of handling tape speeds in the range of 6.25-75.0 inches per second (ips).

The formatter is provided with a selection capability which facilitates the connection of up to two formatters to a single controller. In this configuration one PE and one NRZI formatter may be employed. This provides the capability to mix PE and NRZI transports. Refer to Dual Formatter Specification PERTEC 102090 for operation in this mode.

The formatter operates directly from 100 - 250v ac, single phase, 48 - 400 Hz power. A tapped power transformer facilitates selection of the proper voltage.

1.3 PHYSICAL DESCRIPTION OF EQUIPMENT

Two views of the PE Formatter one shown in Figure 1-1. The complete assembly is designed to be slide-mounted in a standard 19-inch EIA rack.

The formatter can be withdrawn from the rack to within three-quarters of its depth to facilitate servicing. The power supply and printed circuit boards are protected by a perforated panel which can be removed while the unit is extended. This provides access to the printed circuit boards from the top. A swing down front panel (with cutouts to clear the power switch) provides access from the front.

A single operational control, the power switch, is located at the front of the power supply. Power is supplied through a 4-foot strain-relieved cord with a standard 3-pin plug. Interface signals are routed through printed circuit connectors that plug directly into the printed circuit boards.

1.4 FUNCTIONAL DESCRIPTION

The Formatter contains all logic and functions associated with the reading and writing of IBM and ANSI compatible 1600 cpi magnetic tapes.

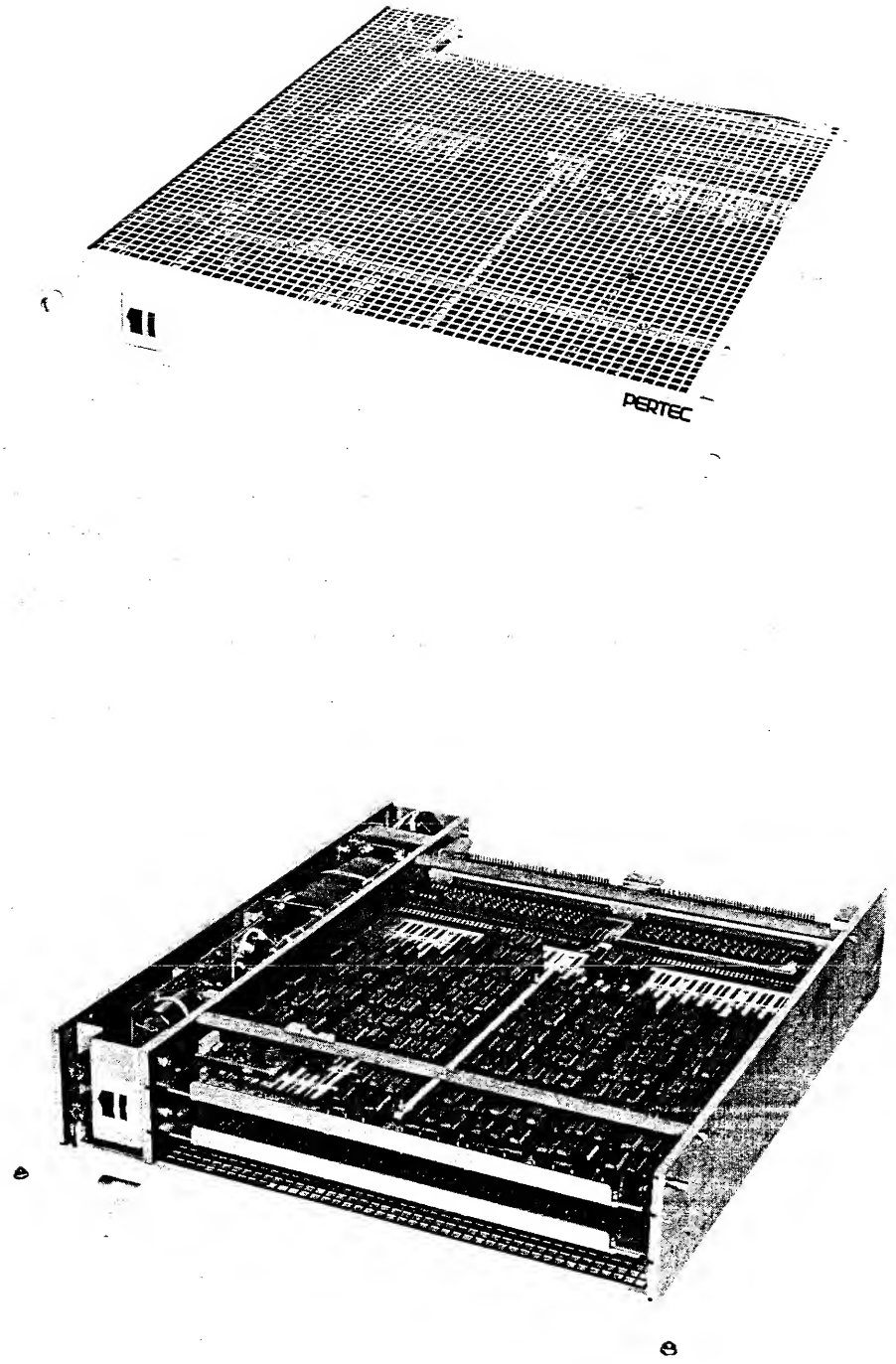


Figure 1-1. Phase Encoded Formatter

All logic for the generation of preamble, postamble, phase encoding data, and file mark patterns for recording onto magnetic tape is included in the formatter. Also, logic for the complete recovery of read data, including data decoding, buffering, error and file mark detection, and error correction logic is included.

Additionally, the formatter includes the following features.

(1) All timing necessary for the generation of IBM compatible IBGs and for correct head positioning between records.

(2) Compatibility with transports having either single or dual stack heads.

(3) Automatic recording of a Phase Mode identification burst prior to recording the first record on a tape.

(4) Automatic testing for the Phase Mode identification burst when reading the first record on a tape.

(5) Provision for fixed and variable length erase commands.

(6) Facility for generation of special commands for the editing of previously recorded tapes.

Two interfaces are provided, one to a controller and another to a tape transport. Two formatters (PE and NRZI in any combination) may be daisy-chained on the controller interface and up to four transports on the transport interface. This provides the capability to employ up to eight transports (NRZI and/or PE) on a single controller. Figure 1-2 illustrates a typical system configuration.

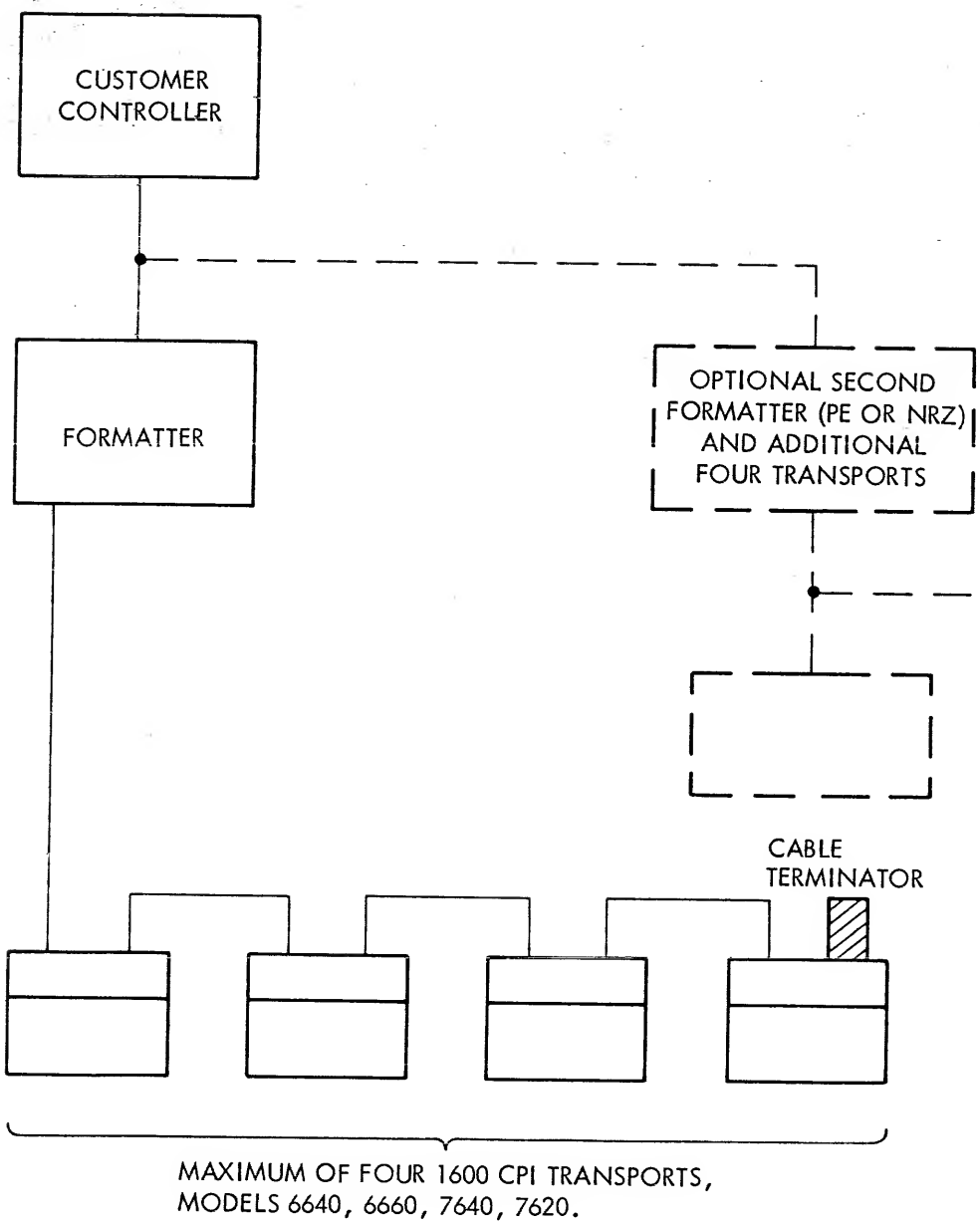


Figure 1-2. PE Formatter System Configuration

1.5 MODEL DIFFERENCES

This manual covers the description of Models F609, F619, F629, and F649. The basic differences between the models are as follows.

(1) Model F649 (Read-after-Write)
Model F629 (Read/Write)
These models are similar except that Model F649 is designed to operate with transports having a dual stack head, and Model F629 is designed for use with transports having a single stack head. Both models consists of three basic sections: control logic, write logic, and read logic.

(2) Model F619 (Read Only)
This model is used in Read Only applications, and consists of two basic sections: control logic, and read logic.

(3) Model F609 (Write Only)
This model is used in Write Only applications, and consists of two basic sections: control logic, and write logic.

The descriptions contained in this manual refer specifically to Models F649 and F629, and should be suitably interpreted when considering the other models.

1.6 MECHANICAL AND ELECTRICAL SPECIFICATIONS

The mechanical and electrical specifications for the formatter are shown in Table 1-1.

Table 1-1
Mechanical and Electrical Specifications

Recording Mode (ANSI, IBM compatible)	PE
Packing Density (cpi)	1600
Number of Channels	9 (8 Data, 1 Parity)
Transport Tape Speed (ips)	6.25 to 75
Data Rate Variation (Tracking Oscillator)	±10%
Deskewing Buffer	Bits per Channel
Preamble	41 Characters
Postamble	41 Characters
ID Burst (1600 frpi)	Channel P
Tape Mark (3200 frpi)	Channels P, 0, 2, 5, 6 and 7
Interblock Gap (IBG)	0.6 Inch (nominal)
Parity	Odd
Dimensions (inches)	
Height	3.5
Width	19.0
Depth	20.0
Weight (pounds)	25 (maximum)
Mounting — Standard 19-inch EIA Rack	—
Power	
Volts (ac)	100 - 250
Watts (maximum)	100
Frequency (Hz)	48 - 400
Electronics	All Silicon
Operating Temperature (°C)	2 to 50
Non-operating Temperature (°C)	-45 to +71
Altitude (feet)	0 to 20,000
Humidity (%)	10 to 95

1.7 INTERFACE SPECIFICATIONS

Levels: True = Low = 0 Volt (approximately)
False = High = +3 Volts

Pulses: Levels as above. Minimum pulsewidth is 1 microsecond. Edge transmission delay over 20 feet of cable is not greater than 200 nano-seconds.

The interface circuits are designed so that a disconnected wire results in a false signal.

Figure 1-3 illustrates the configuration for which the transmitters and receivers have been designed.

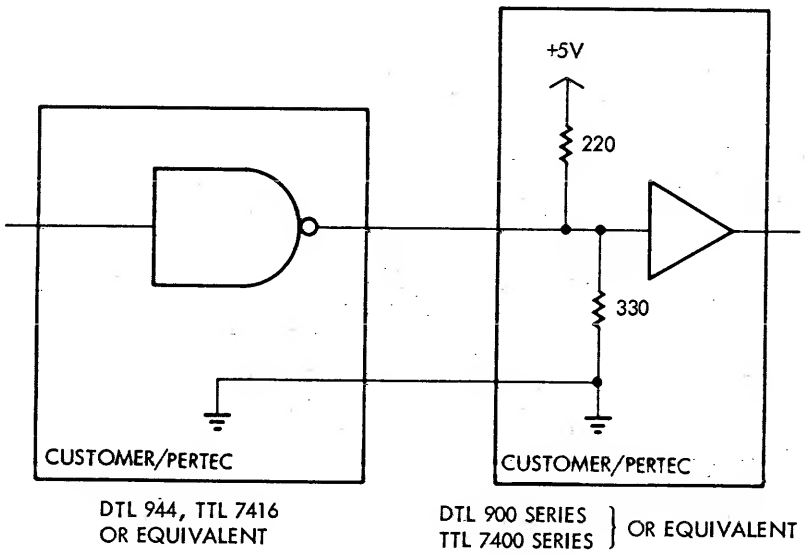


Figure 1-3. Interface Configuration

SECTION II
INSTALLATION

2.1 INTRODUCTION

This section contains a summary of interface lines, information for uncrating the formatter, as well as the procedure for electrically connecting the PE Formatter.

2.2 UNCRATING THE FORMATTER

The formatter is shipped in a protective container built to minimize the possibility of damage during shipping. The shipping container conforms to the National Safe Transit Committee Pre-Shipment Test Procedure.

The following procedure is used to uncrate the formatter unit.

(1) Place the shipping container in the position indicated on the container.

(2) Open the container by cutting the tape along top joints of the container.

(3) Remove four 4- × 4- × 4-inch polyurethane corner blocks.

(4) Remove the entire plywood shipping brace by lifting vertically.

(5) Place the formatter (contained within the shipping brace) on a flat surface and remove four one-fourth-inch steel bolts.

(6) Remove top plywood brace.

(7) Lift the formatter from remaining plywood brace and place on a flat surface.

(8) Remove the formatter from plastic shipping bag.

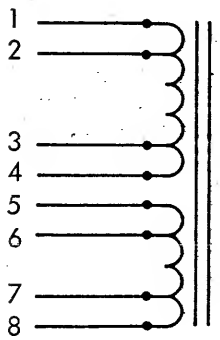
(9) Remove cable and manual from shipping carton.

Check the contents of the shipping container against the packing slip and investigate for possible damage. Notify the carrier immediately if any damage is noted.

Access to the printed circuit boards is obtained by depressing the spring-loaded release button located on the right side of the formatter unit. The front panel, hinged at the bottom, will swing down to allow removal of the polyurethane foam pad placed inside the unit to prevent damage of the printed circuit boards during shipment.

Check the printed circuit boards and connectors for correct seating and installation.

Check that the identification label, located on the inside of the front panel, bears the correct model number and voltage requirement. If the actual line voltage at the installation site differs from that on the identification label, the power transformer taps should be changed as illustrated in Figure 2-1.



LINE VOLTAGE	LINE INPUT	CONNECT
100	2 AND 3	2 AND 6, 3 AND 7
115	2 AND 4	2 AND 6, 4 AND 8
125	1 AND 4	1 AND 5, 4 AND 8
200	2 AND 7	3 AND 6
210	1 AND 7	3 AND 6
220	1 AND 7	3 AND 5
230	2 AND 8	4 AND 6
240	1 AND 8	6 AND 6
250	1 AND 8	4 AND 5

Figure 2-1. Transformer Primary Connections

2.3 POWER CONNECTIONS

A fixed, strain-relieved power cord is supplied for plugging into a polarized 115v ac outlet. For other power sockets, the supplied plug must be removed and the correct plug installed.

2.4 RACK MOUNTING THE FORMATTER

The physical dimensions of the formatter, as illustrated in Figure 2-2, are such that it may be mounted in a standard 19-inch EIA rack; 3.5 inches of panel space is required. A depth of 20 inches behind the mounting surface is required.

To rack mount the formatter, proceed as follows.

(1) Install the two side rails on the formatter using ten No. 8 screws (five per side). Refer to Figure 2-2 for correct positioning.

(2) Install the two side rails in the EIA rack using eight No. 10 screws (four per rail). Refer to Figure 2-2 for correct positioning.

(3) Taking care to align the side guides with the side rails, slide the formatter unit into the rack.

CAUTION

CARE SHOULD BE TAKEN TO ENSURE THAT THE POWER CORD AND INTERFACE WIRING BUNDLES ARE NOT DAMAGED DURING THE RACK MOUNTING OPERATION.

(4) Tighten the two captive retaining screws on the front of the formatter.

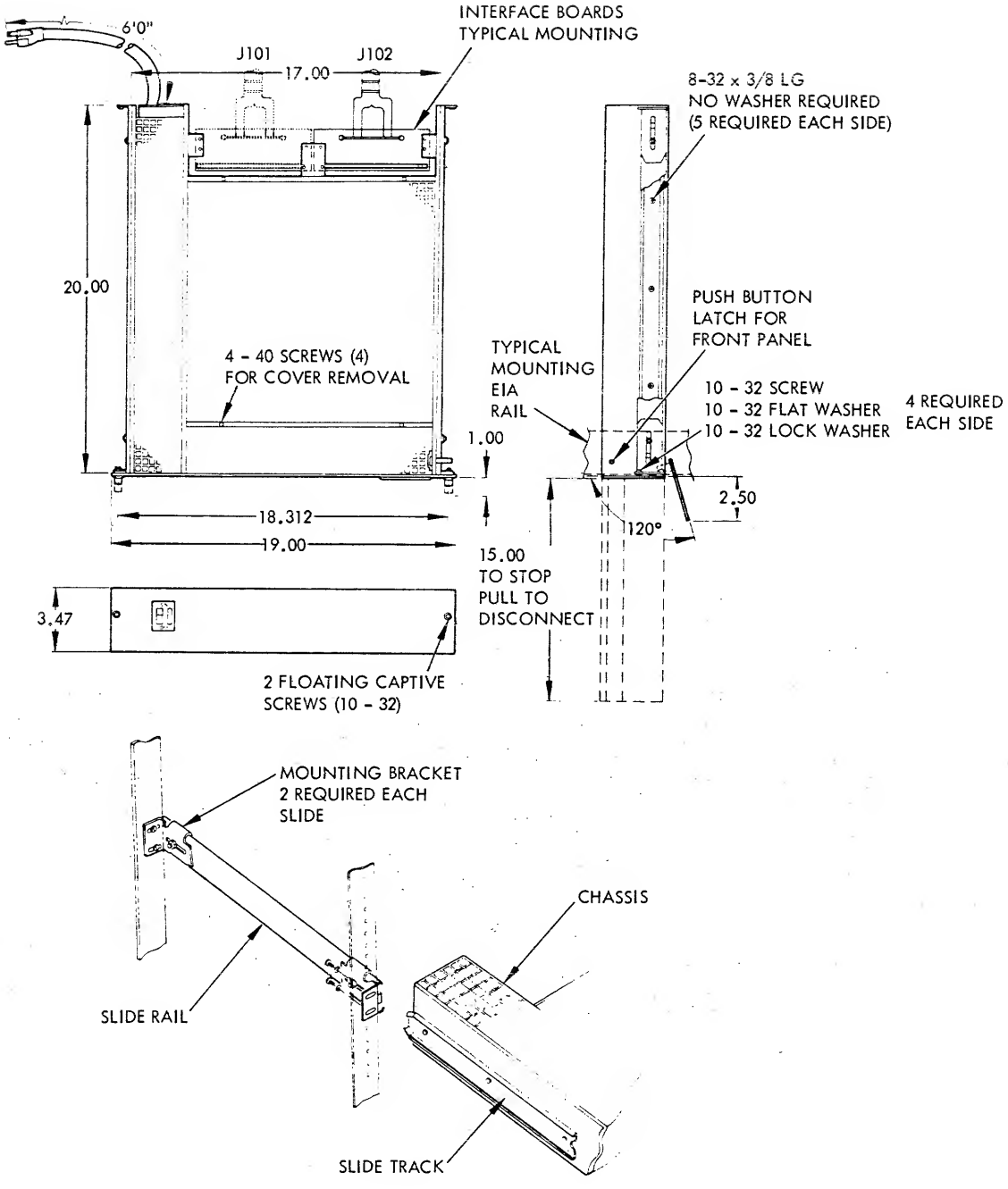


Figure 2-2. Rack Mounting the Formatter

2.5 INTERFACE CONNECTIONS

It is assumed that interconnection of PERTEC Peripheral Equipment and customer equipment uses a harness of individual twisted pairs, each with the following characteristics.

(1) Maximum length of 20 feet.

(2) Not less than one twist per inch.

(3) 22 or 24 gauge conductor with minimum insulation thickness of 0.01 inch.

Ensure that the ground side of each twisted pair is grounded within a few inches of the signal connection.

Included with the formatter is a single input/output cable, five feet in length, which will connect to a transport. This cable is terminated with a strain-relieved edge connector.

The signal connector is a 100 pin 0.1 inch center edge connector, VIKING 2VH50-1JV-5 with a cable terminating board attached. Tables 2-1 and 2-2 list the input/output pin connections.

Table 2-1

Interface Connections, Formatter/Transport

Formatter Connector 101368-01A Mating Connector 2VH50-1JV-5							
Connector (Reference Figure 2-2)	Live Pin	Ground Pin	Signal*	Connector (Reference Figure 2-2)	Live Pin	Ground Pin	Signal*
J102 Transport to Formatter	B1	B2	READ DATA PARITY (RDP)	J102 Formatter to Transport	B15	B14	WRITE DATA STROBE (WDS)
	B3	B2	READ DATA 0 (RD0)		B16	B17	WRITE AMPLIFIER RESET (WARS)
	A3	A2	READ DATA 1 (RD1)		B18	B17	READ THRESHOLD Level 1 (RTH1)
	A6	A5	READ DATA 2 (RD2)		A18	A17	READ THRESHOLD Level 2 (RTH2)
	B7	B8	READ DATA 3 (RD3)		A21	A20	WRITE DATA PARITY (WDP)
	A7	A8	NRZI (NRZ)		B22	B23	WRITE DATA 0 (WD0)
	A9	A8	SINGLE (SGL)		A22	A23	WRITE DATA 1 (WD1)
	B10	B11	SPEED (SPEED)		B24	B23	WRITE DATA 2 (WD2)
	A10	A11	READ DATA 4 (RD4)		A24	A23	WRITE DATA 3 (WD3)
	B12	B11	READ DATA 5 (RD5)		B25	B26	WRITE DATA 4 (WD4)
	B13	B14	READ DATA 6 (RD6)		A25	A26	WRITE DATA 5 (WD5)
	A13	A14	READ DATA 7 (RD7)		B27	B26	WRITE DATA 6 (WD6)
	B36	B35	ON LINE (ONL)		A27	A26	WRITE DATA 7 (WD7)
	A36	A35	REWIND (RWD)		A28	A29	OVERWRITE (OVW)
	B37	B38	FILE PROTECT (FPT)		B30	B29	SYNCHRONOUS FORWARD Command (SFC)
	A37	A38	LOAD POINT (LDP)		B31	B32	SYNCHRONOUS REVERSE Command (SRC)
	A39	A38	READY (RDY)		B33	B32	REWIND Command (RWC)
	B40	B41	END OF TAPE (EOT)		B34	B35	SET WRITE STATUS (SWS)
					A34	A35	OFF-LINE Command (OFC)
					B42	B41	SELECT 0 (SLT0)
					A42	A41	SELECT 1 (SLT1)
					B43	B44	SELECT 2 (SLT2)
					A43	A44	SELECT 3 (SLT3)

* See Section III for definitions of interface functions.

Table 2-2

Interface Connections, Formatter/Controller

Formatter Connector 101368-01A Mating Connector 2VH50-1JV-5							
Connector (Reference Figure 2-2)	Live Pin	Ground Pin	Signal*	Connector (Reference Figure 2-2)	Live Pin	Ground Pin	Signal*
J101 Controller to Formatter	B1	B2	FORMATTER ADDRESS (FAD)	J101 Formatter to Controller	B22	B23	FORMATTER BUSY (FBY)
	A1	A2	TRANSPORT ADDRESS (TAD0)		A22	A23	DATA BUSY (DBY)
	B3	B2	TRANSPORT ADDRESS (TAD1)		B24	B23	IDENTIFICATION (IDENT)
	A3	A2	INITIATE Command (GO)		A24	A23	HARD ERROR (HER)
	B4	B5	REVERSE/FORWARD (REV)		B25	B26	CORRECTED ERROR (CER)
	A4	A5	WRITE/READ (WRT)		A25	A26	FILE MARK (FMK)
	B6	B5	WRITE FILE MARK (WFM)		B27	B26	READY (RDY)
	A6	A5	EDIT (EDIT)		A27	A26	ON LINE (ONL)
	B7	B8	ERASE (ERASE)		B28	B29	REWINDING (RWD)
	A7	A8	READ THRESHOLD LEVEL 1 (THR1)		A28	A29	FILE PROTECT (FPT)
	B9	B8	READ THRESHOLD LEVEL 2 (THR2)		B30	B29	LOAD POINT (LDP)
	B12	B11	REWIND (REW)		A30	A29	END OF TAPE (EOT)
	A12	A11	OFF-LINE (OFL)		A31	A32	NRZI (NRZ)
	B13	B14	LAST WORD (LWD)		A33	A32	SINGLE (SGL)
	A13	A14	FORMATTER ENABLE (FEN)		B34	B35	SPEED (SPEED)
	A15	A14	WRITE DATA PARITY (WP)		A34	A35	WRITE STROBE (WSTR)
	B16	B17	WRITE DATA 0 (W0)		B36	B35	READ STROBE (RSTR)
	A16	A17	WRITE DATA 1 (W1)		A36	A35	READ DATA PARITY (RP)
	B18	B17	WRITE DATA 2 (W2)		B37	B38	READ DATA 0 (R0)
	A18	A17	WRITE DATA 3 (W3)		A37	A38	READ DATA 1 (R1)
	B19	B20	WRITE DATA 4 (W4)		B39	B38	READ DATA 2 (R2)
	A19	A20	WRITE DATA 5 (W5)		A39	A38	READ DATA 3 (R3)
	B21	B20	WRITE DATA 6 (W6)		B40	B41	READ DATA 4 (R4)
	A21	A20	WRITE DATA 7 (W7)		A40	A41	READ DATA 5 (R5)
					B42	B41	READ DATA 6 (R6)
					A42	A41	READ DATA 7 (R7)

*See Section III for definitions of interface functions.

SECTION III
OPERATION

3.1 INTRODUCTION

This section contains the functional specifications of the PE Formatter, a brief outline of the PE tape format, basic formatter operation, and a detailed definition of the various formatter interface lines.

3.2 CONTROLS AND INDICATORS

The formatter utilizes a single operational control located on the front panel.

3.2.1 POWER

The ON/OFF switch is a rocker type switch which connects line voltage to the power transformer. An adjacent indicator provides visual indication of the on/off status of the formatter.

When power is turned on a reset signal is applied to all relevant flip-flops until the power supply voltages have been established.

When power is turned off or line voltage is lost, the formatter will reset all relevant flip-flops before the regulated power supplies decay, thus ensuring that no spurious signals are sent to the transport.

Two twist lock fuses are provided adjacent to the power switch. A 5-amp fast-blow fuse protects the dc circuits and a 1-amp slow-blow fuse protects the ac circuits. Access to the fuses is obtained by opening the hinged front panel of the formatter.

3.3 BASIC OPERATION

The formatter is capable of executing the commands listed in Table 3-1. When a command is received from the customer's controller the formatter goes "busy" and performs all control and timing functions necessary to execute the command. Any errors occurring during the command are reported to the controller. On completion of the command the formatter signals the controller, and the controller is free to issue a further command.

Two other command lines are provided which cause the transport to rewind, or to be switched off-line. These commands are routed directly to the selected transport, and do not cause the formatter to go busy.

Note that for transports having a dual stack head an automatic read-after-write data check is performed during each write command. Read-after-write data is transmitted to the controller in the same manner as during read commands.

Figure 3-1 illustrates the 9-track PE tape format.

Table 3-1
Command Coding

Command	REV	WRT	WFM	EDIT	ERS	THR1	THR2
READ FWD						As Req'd	As Req'd
READ REV (Norm)	X					As Req'd	As Req'd
READ REV (Edit)	X			X		As Req'd	As Req'd
WRITE (Norm)		X					
WRITE (Edit)		X		X			
WRITE FILE MARK		X	X				
ERASE (Variable Length)		X			X		
ERASE (Fixed Length)		X	X		X		

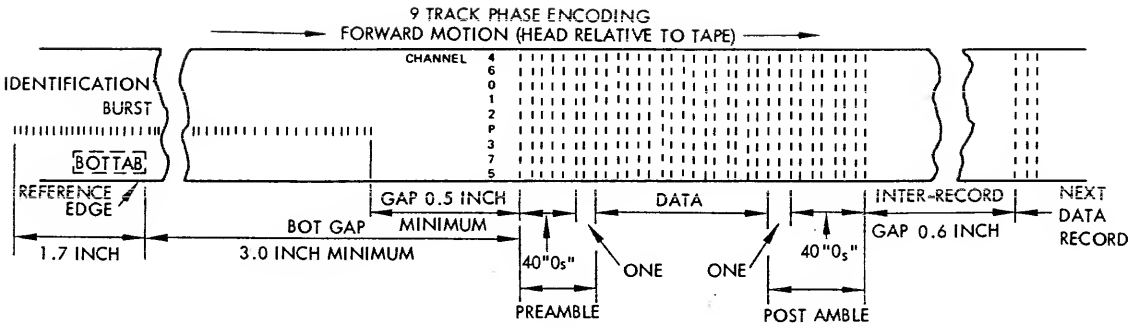


Figure 3-1. 9-track PE Tape Format

3.3.1 PREAMBLE

When writing, the formatter generates a preamble which precedes the data block. The preamble consists of 41 characters; the first 40 characters contain a zero (0) bit in each of the 9 tracks, and the subsequent single character contains a one (1) bit in each of the 9 tracks.

When performing a read operation, the formatter detects the preamble and separates it from the data block.

3.3.2 DATA

When writing, the formatter accepts data, character by character, and converts it into a PE signal in which:

(1) A zero (0) bit is characterized by a transition in the middle of the bit cell away from the erase direction of magnetization.

(2) A one (1) bit is characterized by a transition in the middle of the bit cell toward the erase direction of magnetization.

When reading, the formatter accepts 9 channels of digital phase encoded data from the transport, and provides 4 bits of buffer per channel for the purpose of deskewing. The read logic assembles these data into parallel form, performs various error checks, and transmits the data to the controller on 9 read data lines together with the strobe waveform.

A tracking oscillator is provided in the formatter which can follow data rate variations of up to ±10 percent over 35 character periods. Data rate variation results from the Instantaneous Speed Variation (ISV) in the transport reading the tape, plus the ISV in the transport on which the tape was written.

3.3.3 POSTAMBLE

When writing, the formatter generates a postamble which follows the data and consists of 41 characters. The first character contains a one (1) bit in each of the 9 tracks; the subsequent 40 characters contain a zero (0) bit in each of the 9 tracks.

When performing a read operation, the formatter detects the postamble and separates it from the data block.

3.3.4 IDENTIFICATION BURST

When performing any write operation from BOT, the formatter automatically writes an IBM and ANSI compatible identification mark onto tape. This consists of a sequence of flux reversals at 1600 flux reversals per inch (frpi) in Channel P, with all other channels erased.

A length of tape approximately 3 inches long is then erased before the first data record is written.

In the read mode, the formatter samples the output of the parity channel as the BOT tab traverses the read head. If an identification burst is detected, the IDENT interface line is pulsed.

3.3.5 FILE MARK

When writing, the formatter generates a phase encoded tape mark consisting of 80 flux reversals at 3200 frpi in Channels P, 0, 2, 5, 6, and 7. Channels 1, 3, and 4 are erased in the same direction as the IBG.

When reading, the formatter will recognize a file mark if it contains at least 64 flux reversals in Channels P, 0, and 5, or Channels 2, 6, and 7 with Channels 1, 3, and 4 dc-erased.

3.3.6 GAPS

The formatter provides the timing required to generate the following gaps.

(1) Interblock Gap (IBG)

Nominal	0.6 inch
Minimum	0.5 inch
Maximum	25 feet (depends upon number of consecutive erasures, no restrictions placed by the formatter to limit this distance).

(2) Initial Gap. When writing the first record from BOT, an ID burst is written followed by a gap of approximately 3 inches before the first data block.

When reading, the formatter can detect records written with an initial gap of 0.5 inch minimum between the end of the ID burst and the beginning of the first data block.

(3) File Mark Gap. A file mark is preceded by approximately 3.75 inches of tape with all tracks erased in the same direction as the IBG.

3.3.7 PARITY

During a write operation, the formatter generates odd parity derived from the data present on the 8 data channels. An option is provided (jumper selectable) whereby the parity bit can be supplied externally.

When reading, the formatter checks that the parity of the 9 channels is odd. An error is signalled when the parity check fails.

3.3.8 DROPOUT AND ERROR CORRECTION

The formatter provides single and multiple track dropout detection. When a single track dropout occurs, the formatter performs error correction by use of the parity circuits and the data on the other 8 channels. A status line to the controller indicates when error correction is taking place.

After a track has experienced a dropout, the output of that track will be ignored for the remainder of that record, and no attempt is made to resynchronize the data discriminators on that track.

3.3.9 OPTIONS

The following features are available as options and must be specified at the time of ordering.

(1) Formatter address - "0" or "1"

(2) Internal or external Write Parity generation

(3) Dual speed option

(4) Customer controller mounted in the formatter

3.4 FORMATTER INTERFACING

There are two interfaces provided by the formatter, one from the controller to the formatter, and the other from the formatter to the transport. These interfaces are detailed in Tables 2-1 and 2-2.

The formatter is designed so that any two PERTEC formatters of any type (PE or NRZ) may be daisy-chained on the controller/formatter interface, and up to four transports can be daisy-chained on each formatter/transport interface.

3.5 INTERFACE INPUTS (Controller to Formatter)

All waveform names are chosen to correspond to the logical true condition. All interface lines are low-true at the interface with the true level 0v, and the false level +3v. All pulse widths at the interface must be a minimum of 1 μsecond wide.

A disconnected interface line is interpreted as a logical false signal by the formatter logic.

3.5.1 FORMATTER ADDRESS (FAD)

This is a level which selects one of two possible formatters. A true level on the FAD line selects formatter address 1, a false level selects formatter address 0.

When selected, a formatter is connected to the controller and all controller/formatter interface lines are activated. The individual formatter address is determined by an address switch on the formatter PCBA.

NOTE

The following descriptions of controller/formatter interface lines assume that the formatter is selected, unless otherwise noted.

3.5.2 TRANSPORT ADDRESS (TAD0, TAD1)

The levels on these two lines determine which of the four possible transports is connected to the formatter.

These lines are decoded by the formatter into four individual transport select lines, which are then transmitted to the formatter/transport interface as follows.

TAD0	TAD1	ADDR
0	0	SLT0
0	1	SLT1
1	0	SLT2
1	1	SLT3

3.5.3 INITIATE COMMAND (GO)

This is a pulse which initiates the command specified by the command lines (Paragraphs 3.5.5 through 3.5.11). The information on the command lines is copied into the corresponding formatter flip-flops on the trailing edge of the GO pulse. If the formatter and the selected transport are ready, the command is accepted by the formatter and the FBY signal (Paragraph 3.6.1) is set true.

3.5.4 COMMAND LINES

The levels on these lines specify a command to the formatter. The levels on the command lines are transferred to the formatter on the trailing edge of the GO pulse. The levels must be held steady from 0.5 μsecond before to 0.5 μsecond after the trailing edge of GO.

Table 3-1 defines the command coding for various tape operations. The command lines are identified and functionally described in Paragraphs 3.5.5 through 3.5.11.

3.5.5 REV/FWD (Reverse/Forward)

This is a level which, when true, specifies reverse tape motion and which, when false, specifies forward tape motion.

3.5.6 WRT/READ (Write/Read)

This is a level which, when true, specifies the Write mode of operation and which, when false, specifies the Read mode of operation.

3.5.7 WFM (Write File Mark)

This is a level which, when true and WRT/READ is also true, causes a file mark to be written on the tape.

3.5.8 EDIT

This is a level which, when true during a Read Reverse operation, modifies the read reverse stop delay to optimize head positioning for a subsequent edit operation. When this level is true and WRT/READ is true, the OVW line is activated and the selected transport operates in the Edit mode.

3.5.9 ERASE

This is a level which, when true in conjunction with a true level on the WRT/READ line, causes the formatter to execute a dummy write command.

The formatter will be conditioned to execute a normal write command but no data will be recorded. A length of tape, as defined by LWD (Paragraph 3.5.14) will be erased.

Alternately, if Erase, WRT/READ, and WFM command lines are true, the formatter is conditioned to execute a dummy write

file mark command. A fixed length of tape of approximately 3.75 inches will be erased.

3.5.10 THR1 (Read Threshold Level 1)

The levels on this line are utilized in transports having a single stack head only, and specifies the operating level of the read threshold circuits.

A true level specifies selection of the high read threshold level and a false level specifies the normal read threshold. The true level should be used only when it is required to perform a read-after-write data check.

3.5.11 THR2 (Read Threshold Level 2)

The levels on this line are utilized in those transports having an extra low read threshold capability.

When true, the extra low threshold is specified and, when false, the normal threshold is specified. The true level should be used only when it is required to recover data of very low amplitude.

3.5.12 REW (Rewind)

This is a pulse which causes the selected transport to rewind to the load point. This pulse is routed directly to the transport and does not cause the formatter to go busy.

3.5.13 OFL (Off-Line Command)

This is a pulse which, when true, causes the selected transport to revert to the Off-line mode. This pulse is routed directly to the transport and does not cause the formatter to go busy.

3.5.14 LWD (Last Word)

This is a level which, when true during a Write or Erase (Variable length) command indicates that the next character to be strobed into the formatter is the last character of the record. It is set true by the controller at the time the last data character of the record is placed on the interface lines.

3.5.15 FEN (Formatter Enable)

This is a level which, when false, causes the formatter to reset to the quiescent state. This signal is not gated by FAD (Paragraph 3.5.1); hence, if two formatters are connected to the interface, both will reset simultaneously upon receipt of FEN going false.

This line may be used to disable the formatter if controller power is lost, or to clear the formatter logic in the case of illegal commands or unusual conditions.

3.5.16 W0 - W7, WP (Write Data Lines, Write Parity)

The eight Write Data lines (nine in the case of external Parity option) are utilized to transmit write data from the controller to the formatter. W0 corresponds to the most significant bit, and W7 to the least significant bit of each character.

The first character of a record should be available on these lines less than 40 character periods after DBY (Paragraph 3.6.2) goes true and remain until the trailing edge of the first WSTR (Paragraph 3.6.8) is issued by the formatter. The next character of information must then be placed on these lines within one-half of a character period.

Subsequent characters of a record are processed in this manner until LWD is set true by the controller when the last character is transmitted.

3.6 INTERFACE OUTPUTS (Formatter to Controller)

All waveform names are chosen to correspond to the logical true condition. All interface lines are low-true at the interface with the true level 0v and the false level +3v.

All pulse widths at the interface must be a minimum of 1 μsecond wide.

3.6.1 FBY (Formatter Busy)

This level is normally utilized by the controller to inhibit further commands to the formatter. The level goes true on the trailing edge of GO when a command is issued by the controller and will remain true until tape motion ceases after the execution of the command.

3.6.2 DBY (Data Busy)

This is a level which goes true when the tape on the selected transport has reached operating speed, traversed the IBG and the formatter is about to write a preamble on the tape or look for a read signal from the tape.

DBY remains true until the data transfer is completed and the appropriate post-record delay is completed. DBY goes false as the capstan starts to decelerate the tape.

3.6.3 IDENT (Identification)

This is a level which goes true to identify Phase Encoded (PE) tapes. When reading forward off of the BOT, the formatter inspects the Parity channel for the presence or absence of the identification burst which distinguishes PE tapes.

If an identification burst is detected this line is set true for a short period as the BOT tab passes over the read head.

3.6.4 HER (Hard Error)

This is a pulse or level which, when true, indicates that an uncorrectable read error has been detected by the formatter. This line will be set true for one or more of the following.

(1) False preamble detection

(2) False postamble detection

(3) Buffer overflow

(4) Multi-channel dropout

(5) Parity error without associated channel dropouts.

In all cases except parity error the formatter will cease transmission of further read data and search for the IBG.

When a parity error is detected, the erroneous character will be transmitted and labeled by a pulse on the HER line at RSTR (Paragraph 3.6.9) time.

3.6.5 CER (Corrected Error)

This is a pulse which indicates that a single track dropout has been detected and that the formatter is performing error correction.

NOTE

When performing a read-after-write operation, the record should be rewritten if either a HER or CER error is detected.

3.6.6 FMK (File Mark)

This is a pulse which indicates that the formatter read logic has detected a file mark. This may be during any read forward or read reverse command, or during a write file mark command for a read-after-write transport.

3.6.7 TRANSPORT STATUS AND CONFIGURATION

These lines indicate the status and configuration of the selected transport and are defined exactly the same as in the Transport to Formatter Interface Inputs description (Paragraphs 3.8.1 through 3.8.9) except that they are gated with the formatter address line, FAD.

Status:	RDY, ONL, RWD, FPT, LDP, EOT
Configuration:	NRZ/PE, SINGLE, SPEED

3.6.8 WSTR (Write Strobe)

This is a pulse for each data character to be written on the tape. The Write data lines (WP, W0 - W7) are sampled by WSTR and are copied character by character into the formatter Write logic.

The first character must be available before the first WSTR is generated and subsequent characters must be set up on the lines within one-half of a character period after the trailing edge of each WSTR pulse.

This line will be active during erase (variable length) commands, but data copied into the formatter will have no meaning.

3.6.9 RSTR (Read Strobe)

This is a pulse for each data character read from the tape. The controller logic should sample the read data lines (RP, R0 - R7) at RSTR time.

Individual RSTR pulses will generally be equally spaced although some variation may be present due to skew and bit crowding effects.

3.6.10 RP, R0 - R7 (Read Data Lines)

The nine read data lines transmit read data from the formatter to the controller.

Each character read from the tape is available by sampling these lines in parallel by RSTR. Data remains on RP, R0 - R7 for a full character period. The corresponding RSTR pulse is one-third of a character period wide and is timed to occur during the center of each character period.

3.7 INTERFACE OUTPUTS (Formatter to Transport

All waveform names are chosen to correspond to the logical true condition. All interface lines are low true at the interface with the true level zero volt and the false level +3 volts.

All pulse widths at the interface must be a minimum of 1 μsecond wide.

3.7.1 SLT0 - SLT3 (Transport Select Lines)

The levels on these four lines are utilized to select one transport from the possible four. The levels are generated in the formatter by decoding address lines TAD0 and TAD1 (Paragraph 3.5.2). Only one line can be true at a time.

When a transport is selected, all interface lines to and from the transport are activated and the transport is connected to the formatter.

3.7.2 SFC (Synchronous Forward Command)

This is a level which, when true and the selected transport is ready and on-line, causes the tape to move in the forward direction at the specified speed. When the level goes false, tape motion ceases.

3.7.3 SRC (Synchronous Reverse Command)

This is a level which, when true and the selected transport is ready and on-line, causes the tape to move in the reverse direction at the specified speed. When the level goes false, tape motion ceases.

3.7.4 RWC (Rewind Command)

This is a pulse which, if the selected transport is ready and on-line, causes the transport to rewind to BOT. The RWC pulse is generated within the formatter by gating REW (Paragraph 3.5.12) with FAD (Paragraph 3.5.1).

3.7.5 OFC (Off-Line Command)

This is a pulse which places the selected transport under local control. The OFC pulse is generated by gating OFL (Paragraph 3-28) with FAD (Paragraph 3.5.1). An off-line command can be given while a rewind is in progress provided OFC is separated by at least 1 μsecond from RWC.

3.7.6 SWS (Set Write Status)

The level on this line is the output of a flip-flop within the formatter which identifies the read/write status specified in the last command. The level on this line controls the selected transports read/write electronics. Setting this level true causes the selected transport to enter the write mode of operation. When this level is false, the transport will enter the read mode of operation.

Regardless of the state of the SWS line, the transport will be forced into the read mode of operation under any one of the following conditions:

(1) An RWC or OFC is received

(2) Interlock is lost

(3) Transport is switched to the offline mode.

3.7.7 OVW (Overwrite)

This is a level which, when true, causes special action in the write electronics of the selected transport to facilitate the editing of tapes.

The level is the output of a flip-flop in the formatter logic which stores the condition EDIT as specified in the last command.

3.7.8 RTH1 (Read Threshold 1)

The level on this line is the output of a flip-flop within the formatter which stores the condition of THRI specified in the last command.

When this level is true, and the selected transport has a single stack head, the read electronics of the transport are conditioned to operate in the high read threshold mode. When false, the transport reverts to the normal read threshold.

3.7.9 RTH2 (Read Threshold 2)

The level on this line is the output of a flip-flop within the formatter which stores the condition of THR2 specified in the last command.

The output on this line is used only by those transports which have an extra low read threshold capability. When this level is true, the read electronics of the selected transport are conditioned to operate in the extra low read threshold mode. When false, the transport reverts to the normal read threshold.

3.7.10 WARS (Write Amplifier Reset)

A pulse immediately following the last character of the postamble is generated during all write operations. When in the edit mode this pulse is utilized to control the early turn-off of write current in the selected transport.

3.7.11 WDS (Write Data Strobe)

This is a pulse with a frequency twice the frequency of the data transfer rate. The trailing edge of WDS is utilized to copy the Phase Encoded data appearing on WDP, WD0 - WD7 into the selected transport write logic.

The formatter logic holds the WDP, WD0 - WD7 lines steady for the duration of WDS.

3.7.12 WDP, WD0 - WD7 (Write Data)

These nine lines are utilized to transfer the phase encoded data from the formatter to the selected transport. The information is copied on the trailing edge of each WDS pulse into the selected transport write logic and written directly onto the tape.

3.8 INTERFACE INPUTS (Transport to Formatter)

Waveform names correspond to the logical true condition. All interface lines are low true at the interface with the true level zero volt and the false level +3 volts.

All pulse widths at the interface must be a minimum of 1 μsecond wide.

A disconnected interface line is interpreted as a logical false signal by the formatter logic.

3.8.1 RDY (Ready)

This is a level which is true only when the transport is ready to receive external commands. The following conditions must exist.

(1) All interlocks are made

(2) Initial load or rewind sequence is complete

(3) Transport is on-line

(4) Transport is not rewinding

3.8.2 ONL (On-Line)

This is a level which, when true, indicates that the selected transport is under remote control. This level is false when the transport is off-line and cannot be operated remotely.

3.8.3 RWD (Rewinding)

This is a level which is true when the selected transport is engaged in a rewind operation.

3.8.4 FPT (File Protect)

This is a level which is true when the transport power is on, and a reel of tape without a write enable ring is mounted on the transport.

3.8.5 LDP (Load Point)

This is a level which is true when the BOT tab is located under the photo-tab sensor. The LDP level goes false when the tab leaves the photo-tap sensor.

3.8.6 EOT (End of Tape)

This is a level which, when true, indicates that the EOT reflective tab is positioned under the photo-tab sensor. This level is unsataticised, and transitions to and from the true state are not clean.

3.8.7 NRZ/PE (Transport Format)

This is an optional line which is employed in systems utilizing a mixture of PE and NRZI transports. When true the level indicates that the selected transport is utilizing the NRZI format. When false, this level indicates that the selected transport is utilizing the PE format.

When the level on this line is true, the command lines of a PE formatter are disabled. When the level is false, the command lines of an NRZI formatter are disabled.

3.8.8 SINGLE (Head Configuration)

This is an optional line employed in systems utilizing mixed transports. When true, the level indicates that the selected transport has a single stack Read/Write head. When the level is false a transport having a dual stack read-after-write head is selected.

The levels on this line condition the PE formatter to generate appropriate delays for the generation of the IBG and for head positioning.

3.8.9 SPEED (Tape Speed)

This is an optional line utilized in systems having mixed transports to indicate at which of two possible tape speeds the selected transport is operating.

When false, this line indicates that the selected transport is operating in the High Speed mode. When true, this line indicates that the selected transport is operating in the Low Speed mode.

3.8.10 RDP, RD0 - RD7 (Read Data Lines)

The nine Read Data lines are employed to transmit read data from the selected transport to the formatter. They are the outputs of nine peak detectors, individually gated with the output of a threshold detector associated with each channel. The read signals are replicas of the PE waveforms used to drive the write amplifiers.

SECTION IV

THEORY OF OPERATION

4.1 INTRODUCTION

This section provides a description of the basic organization and operation of the Phase Encoded Formatter.

The formatter consists of the following major components.

(1) Basic hardware

(2) Interconnect 'A' or Interconnect 'B' motherboard

(3) Power supply sub-assembly

(4) PE Write/Control Printed Circuit Board Assembly (PCBA)

(5) PE Read Recovery Printed Circuit Board Assembly (PCBA)

4.2 ORGANIZATION OF THE FORMATTER

A highly modular construction has been adapted with all major sub-assemblies and logic components are interconnected by means of a connector rather than the more conventional wiring techniques.

Although the basic formatter hardware can accommodate up to three PCBA assemblies only two positions are used in the PE formatter. The top slot is utilized for the Read Recovery PCBA, and the bottom slot holds the Write/Control PCBA.

Figure 4-1 illustrates the physical relationship between the motherboard connectors, three card slots and the interface cables in the normal configuration.

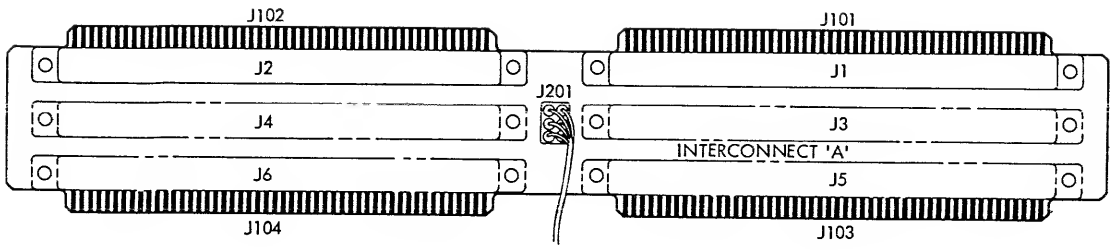


Figure 4-1. Physical Relationship between the Motherboard Connectors, Three Card Slots, and Interface Cables

The PCBAs contain all of the logic required to perform the various formatter functions. Each PCBA consists of a 14 x 16 inches printed circuit board which mates to the Interconnect A motherboard via two 100-pin edge connectors (J1, J2 for the Read Recovery PCBA, and J5, J6 for the Write/Control PCBA). J1 and J5 carry the controller interface signals, and J1 and J6 carry the transport interface signals.

The interconnect motherboard provides for the electrical connection between the three PCBA card slots, and to the two external interfaces. The edge connector sockets associated with the controller interface (i.e., J1, J3, and J5), are daisy-chained together and then routed to edge connectors J101 and J103. External connection to the controller is usually made via J101.

Similarly, the motherboard sockets associated with the transport interface (J2, J4, and J6) are daisy-chained together and routed to edge connectors J102 and J104. Connection between the formatter and transport is made by use of the Cable "A" assembly which is shipped with the formatter. This cable mates to the formatter via J102.

NOTE

Pins on the 100-pin connectors are numbered

A1 - A50

B1 - B50

where pin A1 is opposite B1, etc. Due to the topology of the motherboard, pin connections on the four external interface connectors are reversed at the PCBA connectors (e.g., the waveform GO appears on pin A3 for interface connectors J101 and J103, and on pin B3 for PCBA connectors J1, J3, and J5).

When making external connections, refer to Table 2-1 (Transport Interface) and Table 2-2 (Controller Interface). Definitions of the interface signals are contained in Section III.

The Interface 'B' motherboard is employed only when it is required to mount the customers' controller in the formatter assembly. For this configuration the Write/Control PCBA is moved to the middle card slot, and the controller is mounted in the bottom slot. Surplus formatter power of 5v dc at 2 amps is available to drive the controller logic.

The Interface 'B' motherboard is similar to the Interface 'A' motherboard except that the etched interconnections between J4 and J6 are removed. The controller will interface to the formatter PCBAs via J5, and to external equipment via J6 and J104.

DC power is delivered from the Power Supply sub-assembly to the motherboard via connector J201. The motherboard distributes power to each of the PCBA card slots through connectors J1 through J6.

4.3 FUNCTIONAL DISCUSSION

4.3.1 POWER SUPPLY

Figure 4-2 is a block diagram of the power supply, which is located along the left side of the main assembly. The transformer, fuses, rectifiers, and power card, etc., are fastened directly to the power supply sub-assembly. The switching regulator, over-current detector, over-voltage detector, and the logic enable circuitry are located on a PCBA which is mounted in the power supply sub-assembly.

The power supply sub-assembly supplies +5v dc and a logic enable signal, PSEN, to the formatter logic. A switching regulator converts unregulated +20v to a +5 v supply which is rated at 8 amps. The supply is protected from overloads by a current limiter.

NOTE

In the case of an overload condition the +5v supply will be removed from its load by the over-current detector. To reset the detector, ac power must be shut off for approximately 60 seconds.

The formatter logic is also protected from excessive voltage by an over-voltage detector which blows the dc fuse if the supply voltage exceeds +7.5v.

A reset signal, PSEN, is generated in the power supply and is used to clamp all formatter logic to the quiescent state while dc power is being established after switch-on. Similarly, when ac power is lost, PSEN clamps for formatter logic before there is a significant decay in the +5v supply and prevents the writing or reading of spurious signals.

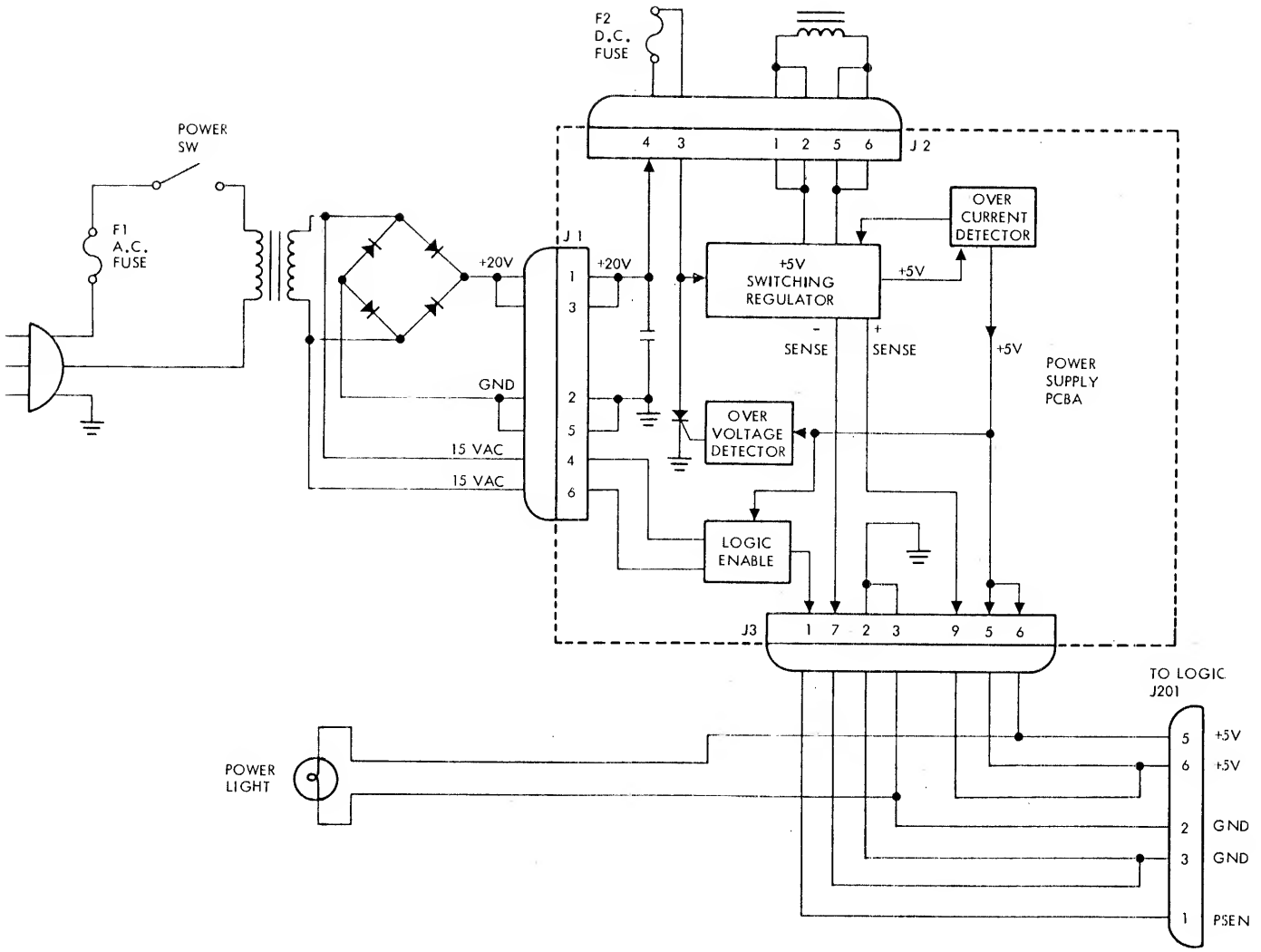


Figure 4-2. Block Diagram, Power Supply Sub-Assembly

4.3.2 PE FORMATTER PCBAs

All logic necessary to perform the various formatter functions are contained on two IC logic assemblies, the Write/Control PCBA and the Read Recovery PCBA.

Each PCBA contains an oscillator which controls the timing of all waveforms on the PCBA. On the Write/Control PCBA this is a fixed frequency oscillator, and on the Read Recovery PCBA it is a tracking oscillator.

Both oscillator frequencies are initially adjusted according to tape speed. Different tape speeds can therefore be easily accommodated by a simple change in oscillator frequency. Dual speed oscillators are also available which allow transports of two different speeds to be attached to the same formatter.

The formatter logic must be conditioned according to the type of transport in use. This is accomplished by use of the three configuration lines on the transport interface, as follows.

(1) NRZ/PE: distinguishes between NRZ and PE transports. This line must be held false when using the PE formatter.

(2) Single/Dual: defines whether transport has a single stack (read/write) or dual stack (read-after-write) head.

(3) Speed: for PE formatters having a dual speed capability, this line selects one of two possible tape speeds.

When the formatter is dedicated to one type of transport the configuration lines are usually hardwired to the appropriate condition by jumber wires on the formatter PCBAs.

Alternately the configuration lines may be controlled by the output from the selected transport. This permits transports of different configurations to be daisy-chained onto the same formatter.

4.3.3 WRITE/CONTROL PCBA

The Write/Control PCBA contains all logic necessary to perform all formatter functions except read recovery.

Formatter interface connections are illustrated in Figure 4-3. A simplified block diagram of the Write/Control logic is shown in Figure 4-4 and should be referred to for the following discussion.

4.3.3.1 Control Logic

Performance of any formatter operation is dependent upon the formatter being selected by the controller. The formatter address is specified by the Formatter Address (FAD) and a logical comparison is made against the position of an address switch on the PCBA. When a true comparison is made the formatter is connected to the controller interface.

When selected, the formatter will subsequently respond to controller commands provided no other reset condition exists. Transport address lines TAD0 - TAD1 are decoded and the selected transport is enabled. Status and configuration information from the selected transport will be routed to the controller via the formatter.

Note that Rewind and Off-line commands (REW and OFL) are routed directly to the selected transport and are active any time the formatter is selected.

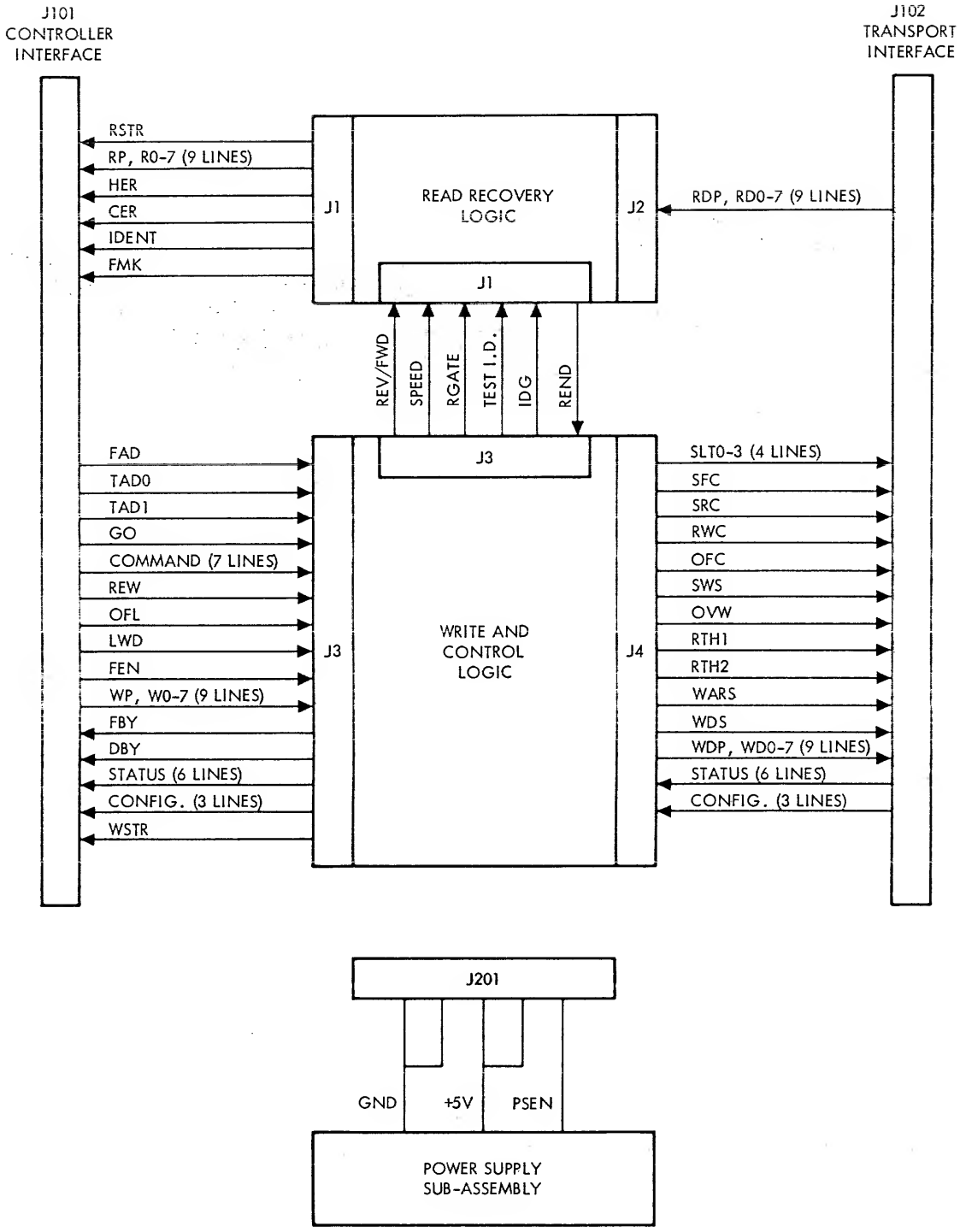
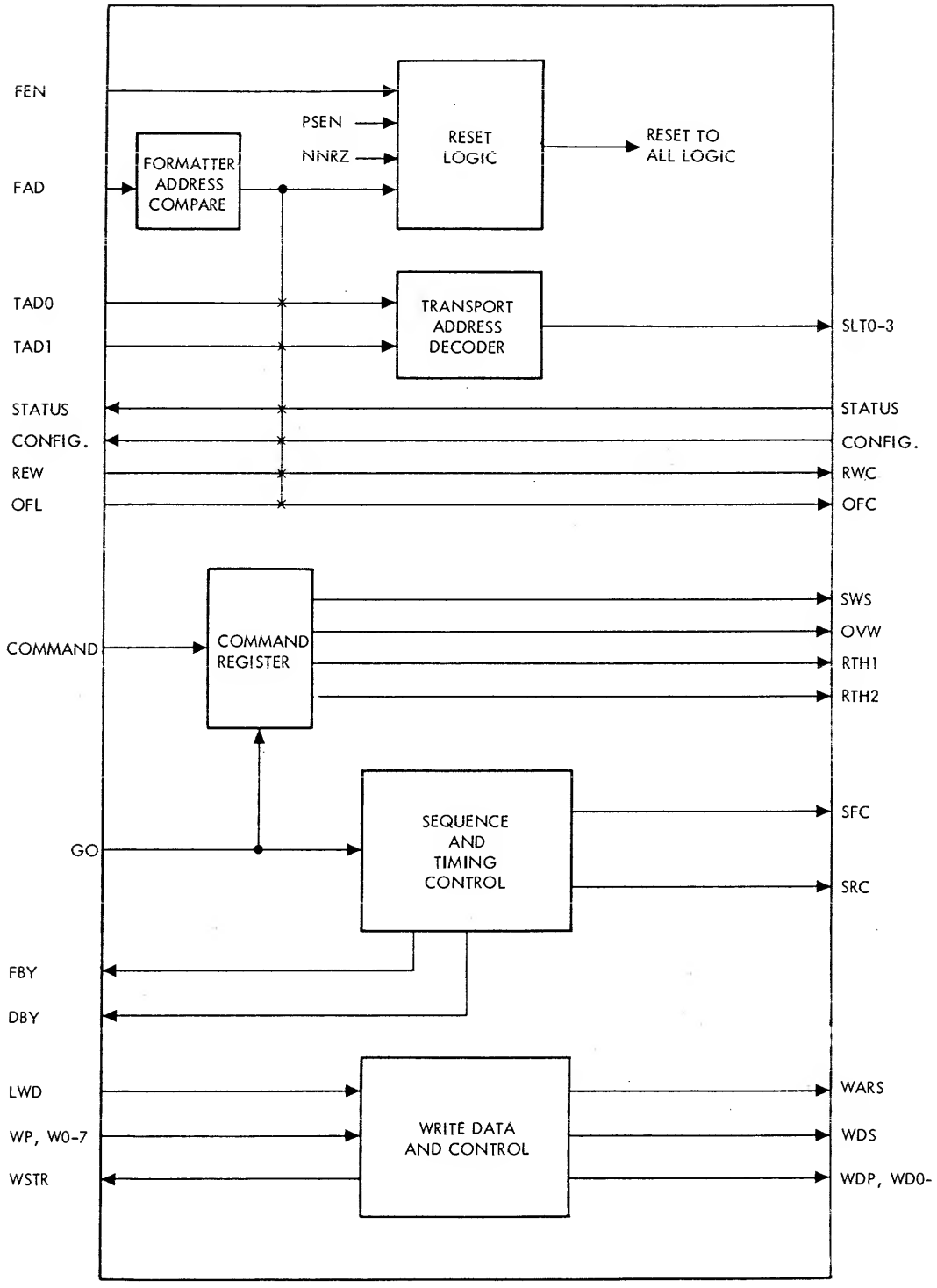


Figure 4-3. Organization of the Phase Encoded Formatter



* INDICATES LINE IS GATED BY FAD

Figure 4-4. Write/Control Logic, Simplified Block Diagram

All other commands require that all inputs to the reset logic be true, i.e., the formatter is selected, power is established, no external reset from the controller is present, and the selected transport is compatible with the formatter.

To initiate a command, the seven command lines are set according to Table 3-1 and the GO line is pulsed. If no reset condition exists, the formatter is not busy, and the selected transport is ready, the command is accepted by the formatter.

The information on the command lines will be copied and stored in a command register on the trailing edge of the GO pulse. Formatter Busy (FBY) will be set true and the formatter will begin the timing and sequencing required to execute the command.

At the end of a pre-record delay which allows the transport to ramp up to speed and traverse the IBG, Data Busy (DBY) is set true and the read and/or write logic is activated. Data transfer will now take place between Controller/Formatter/Transport as specified by the command.

At the conclusion of the data transfer a post-record delay is initiated which either assists in the generation of IBM-compatible gaps or optimizes head positioning within the gap. DBY goes false at the end of the delay period and a stop command is given to the transport. FBY will remain true while the transport is ramping down and will reset when the tape velocity reaches zero.

4.3.3.2 Command Separation

In most formatter applications it will be sufficient for the controller to inhibit execution of a new command until after the trailing edge of FBY. This means that the transport will always ramp down to a halt between commands.

However if maximum performance is required, the formatter can be operated in the "on-the-fly" mode. In this mode the controller is allowed to issue a new command anytime after DBY goes false, provided that the following conditions are met:

(1) The new command is in the same forward/reverse direction as the previous command. This ensures the integrity of the transport stop/start times and distance.

(2) The new command is in the same Read/Write mode of the previous one. This prevents the possibility of unerased areas of tape being left in the IBG.

The controller must furnish the logic necessary to detect these two conditions. "On-the-fly" operation results in a maximum time saving of one start/stop time per command (e.g., 30 ms/command at 12.5 ips).

4.3.3.3 Write Data and Control Logic

The Write Data and Control Logic, located on the Write/Control PCBA, controls the execution of all commands which involve the writing of data or the erasing of data from tape; i.e., Write (normal), Write (edit), Write File Mark (WFM), Erase (variable length) and Erase (fixed length).

Figure 4-5 illustrates the sequence of events in the execution of a typical write command. Note that the write logic is activated after tape has ramped up to speed and the correct IBG has been written.

4.3.3.4 Write (Norm), Write (Edit)

The Write (Norm) and Write (Edit) commands are executed in an identical manner by the write logic. In the case of a Write (Edit) operation the EDIT Command line is held true causing the OVW flip-flop to set. Setting OVW causes the write electronics in the selected transport to operate in the edit mode.

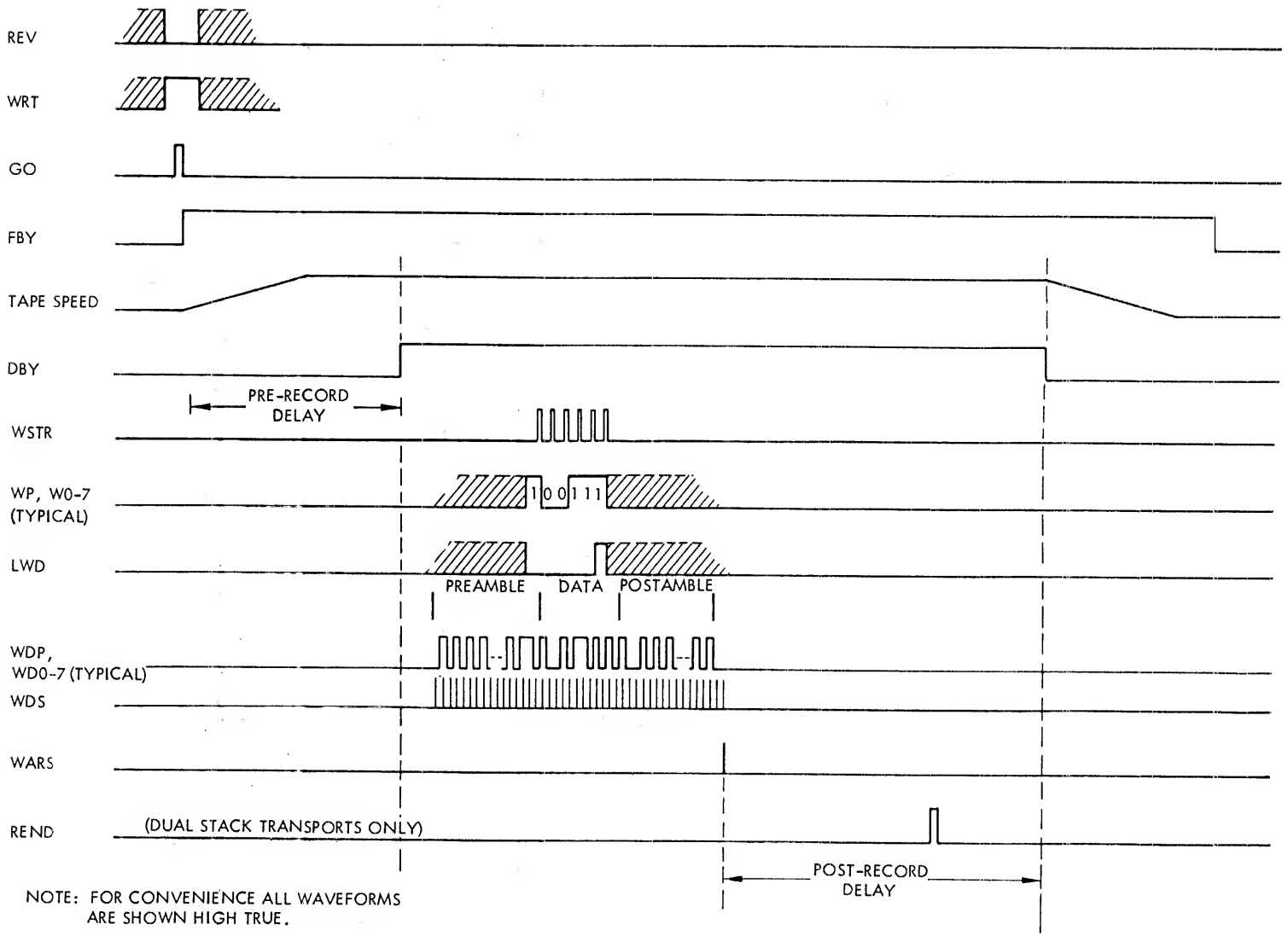


Figure 4-5. Phase Encoded Write Operation

When DBY goes true (Figure 4-5) the formatter write logic begins to generate a preamble data pattern consisting of forth "0" bits followed by a "1" bit. This pattern is phase encoded, then written simultaneously onto the nine data channels on tape.

During the time period in which the last preamble bit (1) is being recorded, a WSTR pulse is issued to the controller.

On the trailing edge of WSTR the data appearing on WP, W0-7 is copied into the formatter, encoded, and then written onto tape immediately following the preamble "1" bit.

The controller should use the trailing edge of the WSTR pulse to set the next byte of data on WP, W0-7. The formatter requires that the first bit be set up on the data lines before the first WSTR is issued and that the subsequent bits are set up within one-half of a character period after the trailing edge of WSTR.

The controller will set LWD true when the last data byte is set on WP, W0-7. When the following WSTR pulse occurs the formatter samples LWD and will then enter a postamble sequence immediately following the writing of the last data byte.

The postamble pattern is a mirror image of the preamble and consists of a "one" bit followed by 40 "zero" bits. The postamble is phase encoded and written simultaneously on the nine tape tracks.

Shortly after the last postamble bit is recorded a Write Amplifier Reset (WARS) pulse is issued by the formatter. The WARS pulse is employed in some tape transport models to control write current turn-off at the end of an edit operation.

When operating with a transport utilizing a single stack head the post record delay is initiated immediately after the last postamble bit is recorded.

The write sequence is terminated in a different manner when operating with a dual stack transport. The post-record delay is not initiated immediately after the last postamble bit is recorded. The delay is initiated after the transports read electronics has completed read-after-write check on the data just recorded. An internal waveform, REND, is utilized to indicate the end of the read-after-write operation.

Following the post record delay DBY goes false and a stop command is given to the transport.

Finally, FBY is reset shortly after the tape comes to rest.

4.3.3.5 Writing from BOT

The 1600 cpi PE format requires that tapes which are recorded in the Phase Encoded mode be identified by a burst of alternate ones and zeros at the BOT marker. It is also required that the first record be written approximately 3 inches after the marker.

When writing from BOT the formatter generates an extra long pre-record delay. In a suitable time interval during the delay the PE identification burst is written consisting of a pattern of alternate ones and zeros (1 0 1 0 1 0 1 0) in the Parity Channel. All other channels are erased.

Upon completion of the pre-record delay the tape is positioned approximately 3 inches past the BOT marker and the first record is now written in the normal manner.

4.3.3.6 Write File Mark

A file mark record consists of at least 80 flux reversals at 3200 frpi in Channels P, 0, 2, 5, 6, and 7. Channels 1, 3, and 4 are dc erased. The file mark is separated from the preceding record by approximately 3.75 inches, and from the following record by a nominal IBG (0.6 inch).

The formatter generates a long pre-record delay equivalent to a 3.75-inch IBG. The write logic then generates and encodes 40 preamble "zero" bits and records this onto Channels P, 0, 2, 5, 6, and 7. This pattern is equivalent to 80 flux reversals at 3200 frpi. The postamble "one" bit is not recorded.

At the completion of the write file mark operation the command is terminated in the same manner as other write operations.

4.3.3.7 Erase (Variable Length)

The Erase (Variable Length) is a dummy write command and is used to erase any desired length of tape. This operation is useful in applications which require the ability to erase individual records on a previously recorded tape.

In executing the Erase (Variable Length) command the formatter performs all operations of a normal write command except that the dummy data being transmitted from the controller to the formatter is not recorded. Therefore, a length of tape equivalent to the dummy record is erased. The LWD signal determines record length in the manner previously described.

4.3.3.8 Erase (Fixed Length)

The Erase (Fixed Length) command is a dummy Write File Mark command. When executed, a fixed length of tape (approximately 3.75 inches) is erased.

4.3.4 READ RECOVERY PCBA

The Read Recovery PCBA illustrated in Figure 4-6 contains the logic necessary to perform the formatter function of read recovery. These functions are Read Forward, Read Reverse (Normal) and Read Reverse (Edit). It is also utilized in performing simultaneous read-after-write data checks when utilized with transports having dual stack heads.

The read recovery logic is activated by the control waveform, RGATE, from the Write/Control PCBA. RGATE goes true at the end of the pre-record delay. Upon reading a complete record, a REND pulse is transmitted back to the Write/Control PCBA which resets RGATE. The re-setting of RGATE deactivates the Read Recovery PCBA.

4.3.4.1 Tracking Oscillator

The tracking oscillator is located on the Read Recovery PCBA. It compensates the read logic timing for instantaneous or average tape speed variations of both the transport which wrote the tape and the transport that is performing the read function.

The tracking oscillator servos on one data channel such that its frequency is always a fixed multiple of the data rate. If the channel happens to suffer a dropout the tracking function is automatically switched to another track.

4.3.4.2 Read Data Channel Logic

There are nine identical channels of read logic which operate independently of each other. Figure 4-7 illustrates a typical Read Data Channel. Incoming data is routed to a circuit which either inverts the data or not, dependent on whether the transport is reading tape in the forward or reverse direction. The purpose of this is to ensure that any given flux transition on tape appears as the same change in signal polarity.

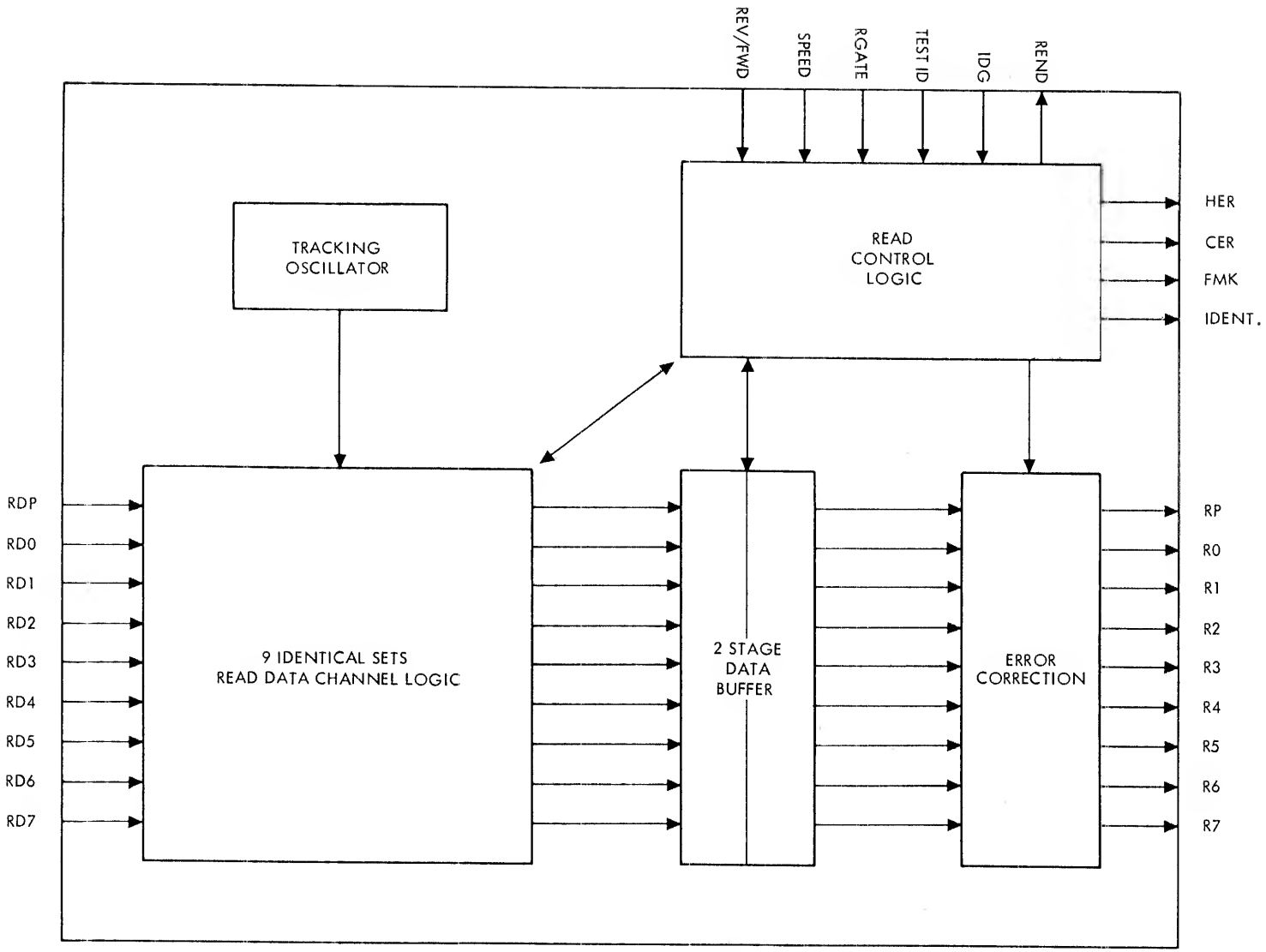


Figure 4-6. Read Recovery PCBA, Simplified Block Diagram

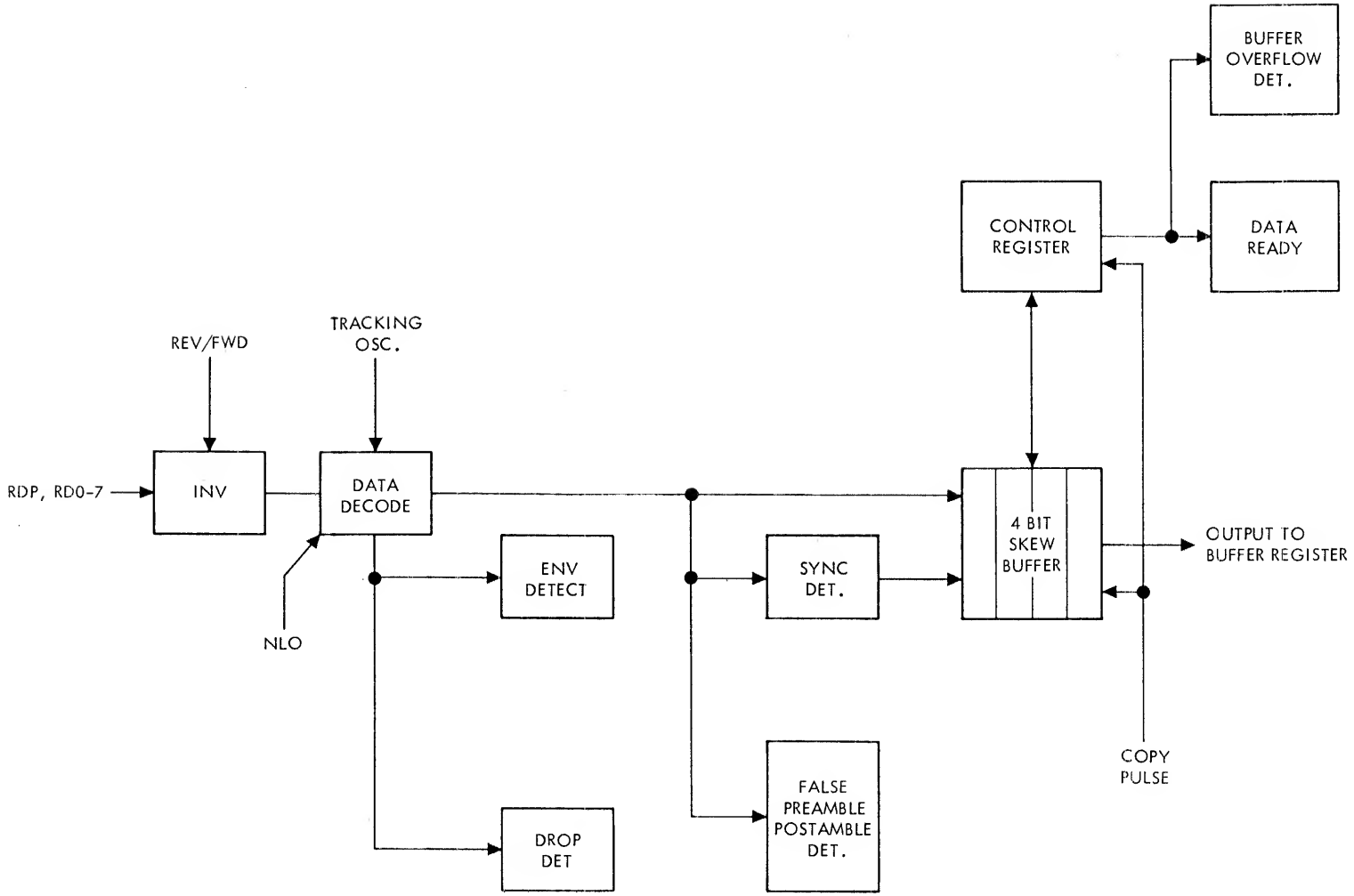


Figure 4-7. Read Data Channel Logic

The remainder of the read recovery logic operates independetly of tape direction.

The output of the inverter circuit is fed to a data decoder whose purpose is to distinguish each bit cell from the next and to decode the data contained within each cell.

Associated with the decoder is an envelope detector which continuously senses the presence (or absence) of data. A dropout detector monitors the data decoder during certain portions of each record and sets a flag if dropout occurs.

The decorder is forced to lock onto the correct signal edge during the first period of the preamble by the NLO signal. During the same period the tracking oscillator will track onto the instantaneous data rate from its center frequency.

When lockon is achieved, NLO is released and the dropout detector is enabled. False preamble checks are now made and the logic then waits for the first "one" bit. When received, the "one" bit is interpreted as being the "one" bit written at the end of the preamble and will cause the SYNC flip-flop to set. All following bits until postamble detection will be interpreted as data bits.

The first data bit is copied into a four-bit skew buffer. The control register simultaneously shifts left one place to record the occurrence. If this bit is still present when the second bit arrives, the second bit will be copied into the second position of the buffer. The amount of skew buffering actually used during a data transfer depends upon the combined write and read misalignments between the 9 channels, and is typically less than half of the four bits provided for by the formatter. In the case of excessive skew a buffer overflow detection circuit will operate if the capacity of the skew buffer is exceeded.

A COPY pulse is issued when the read control logic detects that all 9 data channels have a bit ready. This causes the first byte of data (now in parallel) to be copied into the first stage of the data buffer, and the contents of the first stage to be copied into the second stage etc. Simultaneously each of the skew buffers and control registers are shifted right one place to make room for new data.

4.3.4.3 Read Logic Control

The Read Logic Control circuits exercise overall control over the Read Recovery PCBA. Refer to Figure 4-6 for the following discussion.

4.3.4.4 Sequencing and Timing

This portion of the Read Logic control circuits detect the presence of data from tape and supervises the sequence of events necessary to read a record. Functions include lock-on, timing for preamble and postamble tests, detection of data available in the skew buffers, postamble detection, and end of record detection (REND).

4.3.4.5 Error Detection

During a read operation, a comprehensive set of tests are made to ensure that each record meets 1600 cpi format requirements and that the data is error free. These tests are:

(1) Single channel dropout

(2) Multi-channel dropout

(3) False preamble detection

(4) False postamble detection

(5) Buffer overflow

(6) Parity error without associated channel dropout

In the case of a single channel dropout (1), error correction is performed automatically. Data from the channel suffering a dropout is discarded and replaced by regenerated data which has been computed on the basis of data on the other eight channels together with the parity circuits. Interface waveform, CER, indicates to the controller that error correction is taking place.

All other error conditions are not correctable and will result in a hard error indication, HER, to the controller. Note that for cases (2), (3), (4), and (5) transmission of data to the controller ceases immediately upon detection of the error. For case (6), data transmission will continue, and each byte in error will be labelled by a pulse on HER at the time the corresponding RSTR is issued.

4.3.4.6 File Mark Detection

A test for file mark is made at the time lockon is removed, about midway through the preamble. If the record contains data in Channels P, 0, and 5, or Channels 2, 6, and 7, with Channels 1, 3, 4 erased, the record will be recognized as being a file mark. Interface line, FMK, indicates to the controller that a file mark has been detected.

4.3.4.7 Ident Detection

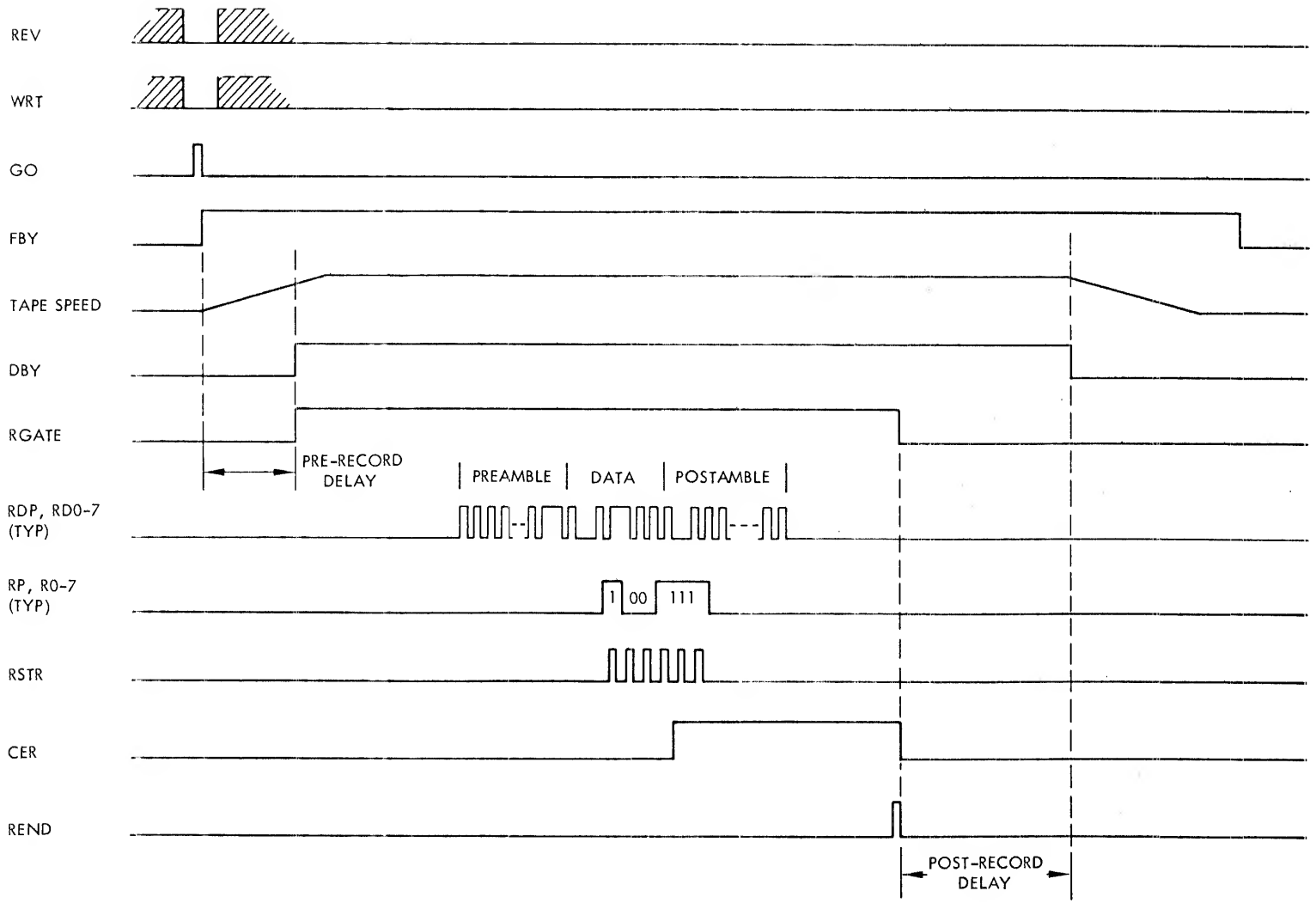
When reading off BOT a test is automatically made to verify the presence or absence of a 1600 cpi identification burst at the BOT marker. As the BOT tab moves over the read head a control signal, IDG, generated in the Write/Control PCBA goes true and activates the envelope detector portion of the read data channels.

Shortly afterwards the TEST ID line is pulsed, and samples the state of the envelope detectors. If Channel P contains data and all other channels are dc erased, the IDENT interface line is pulsed.

For transports having a dual stack head, IDENT detection is also operative when writing from BOT.

4.3.4.8 Read Waveforms

Waveforms for a typical read operation are shown in Figure 4-8.



NOTE: FOR CONVENIENCE ALL WAVEFORMS ARE SHOWN HIGH TRUE.

Figure 4-8. Phase Encoded Read Operation Illustrating Error Correction for Last Two Data Bytes

SECTION V
DETAILED ELECTRICAL AND LOGIC DESCRIPTION

5.1 INTRODUCTION

This section consists of a detailed description of the operation of the formatter logic PCBAs, oscillator, and power supply assemblies. Relevant schematic and assembly drawings are contained at the end of Section VII. Reference should be made to the Theory of Operation, Section IV, for a discussion at the block diagram level.

Before proceeding, it will be useful to list some of the conventions that have been adopted concerning waveform names, logic levels, and logic symbols.

5.1.1 INTERNAL FORMATTER SIGNALS

The formatter logic levels are 0v and +4v (approximately).

The basic waveform names within the formatter have been chosen to correspond to the high-true condition (e.g., the waveform WRT is at +4v when writing, and at 0v when not writing).

The inverse waveform (low-true equivalent) usually retains the same basic name, but is prefixed by the letter "N", e.g.,

WRT	NWRT	
+4v	0v	when writing
0v	+4v	when reading

Logic signals which perform gating functions are identified at the gate in the form which will satisfy the gate logic.

5.1.2 INTERFACE SIGNALS

All signals on the Controller/Formatter and Formatter/Transport interfaces are low-true with signal levels of +3v false, and 0v true. The false level of +3v is determined by a 220/330-ohm resistor chain which terminates each line at the receiver end.

Interface waveform names are always prefixed by the letter "I", e.g., IWRT.

5.1.3 LOGIC ELEMENTS AND SYMBOLS

The formatter logic is designed around the TTL 7400 series, and DTL 800 series of integrated circuit (IC) elements. The ICs on each PCBA are arranged in a grid array with each location identified by row (letter) and column (number). The symbol for each logic element includes the appropriate grid reference and identifies each input and output pin.

Two different types of gating elements are employed; the high-true NAND, and the high-true NOR. Both types consist of a gating function followed by an inversion.

The high-true NAND (e.g., 7400, 7420, 7440, 844) can be used as a NAND gate for high-true inputs, or as a NOR gate for low-true inputs. Similarly, the high-true NOR (e.g., 7402) can be used as a NOR gate for high-true inputs, or as a NAND gate for low-true inputs.

The logic symbols shown on the schematic correspond to the logic function that each gate provides in the circuit. Figure 5-1 illustrates the logic symbols for the 7400 and 7402.

Further descriptions in this manual will refer to gates simply as NOR or NAND, without regard to signal polarity. The presence or absence of circles (state indicators) at the gate inputs indicate the element type.

Also, when it is necessary to refer to a particular element or to a signal having no waveform name, it will be identified by the appropriate output pin number (e.g., C3/3).

Other conventions, illustrated in Figure 5-2, are a double line on the symbol to indicate heavy drive capability. A cross at the output is added to indicate an open collect output.

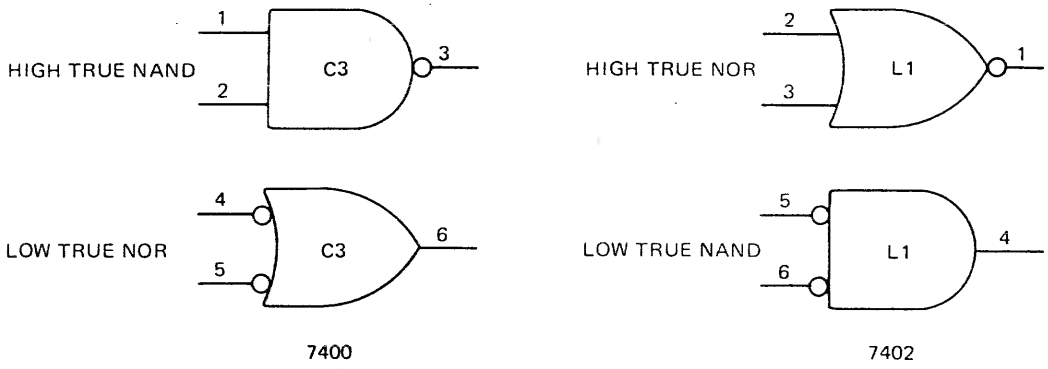


Figure 5-1. Logic Symbols, 7400 and 7402

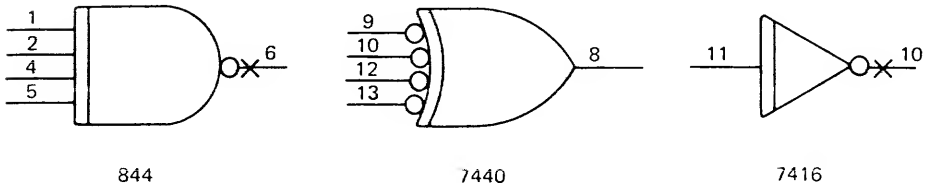
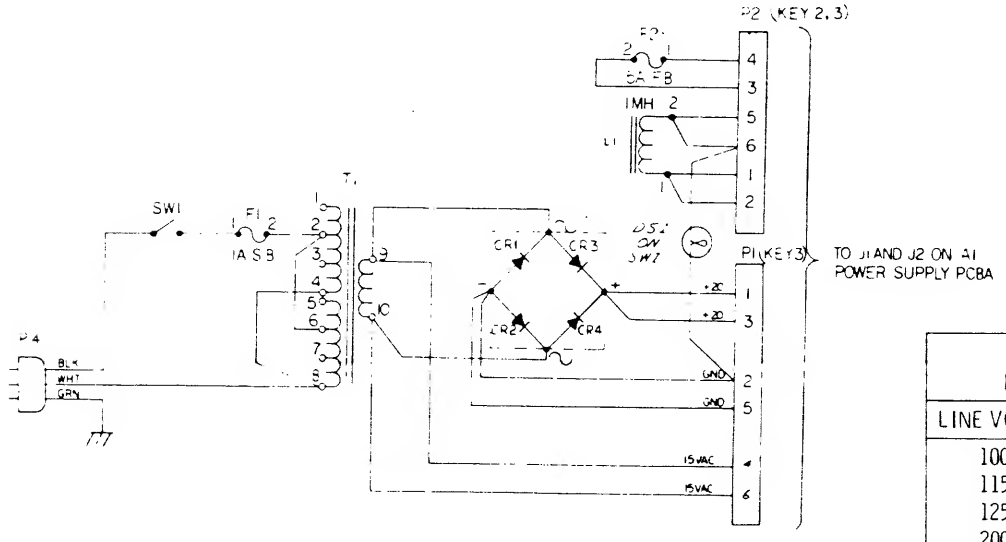


Figure 5-2. Logic Symbols, 844, 7440, and 7416

5.2 POWER SUPPLY ASSEMBLY

The power supply assembly is mounted on the left side of the formatter and generates a dc supply of +5v at 8 amps to drive the formatter logic PCBAs. The assembly is completely self-contained, and can be separated from the rest of the formatter by removal of 4 screws on the center card support.

Major components such as the transformer, bridge rectifier, power switch, etc., are mounted directly to the side support. These components are wired together and connect to a printed circuit board through two molex connectors, P1 and P2. Transformer taps are provided for line voltages in the range 100v - 250v ac. Figure 5-3 illustrates the circuitry and transformer tap connections.



TERMINAL CONNECTORS FOR LINE VOLTAGE VARIATIONS		
LINE VOLTS	LINE INPUT	CONNECT
100	2 AND 3	2 TO 6 AND 3 TO 7
115	2 AND 4	2 TO 6 AND 4 TO 8
125	1 AND 4	1 TO 5 AND 4 TO 8
200	2 AND 7	3 TO 6
210	1 AND 7	3 TO 6
220	1 AND 7	3 TO 5
230	2 AND 8	4 TO 6
240	1 AND 8	4 TO 6
250	1 AND 8	4 TO 4

Figure 5-3. Chassis Mounted Power Supply Components

5.2.1 POWER SUPPLY PCBA

The power supply printed circuit board is mounted on the formatter power supply assembly. Schematic No. 101335 and Assembly No. 101336 should be referred to for the discussions which detail the functions of the formatter PCBA in the following order.

(1) +5v Regulator

(2) Overcurrent Protection

(3) Overvoltage Protection

(4) Logic Enable

5.2.1.1 +5v Regulator

The +5v regulator is a switching regulator which converts unregulated +20v to regulated +5v. The switching is performed by Q8 and its drivers Q5, Q6, and Q7. The +SENSE and -SENSE are tied to the +5v and ground lines respectively at the load for remote sensing. The voltage across the load is compared with a reference voltage generated by the zener diode CR3 and divided by potentiometer R4. When the voltage on the base of Q4 is less than the voltage on the base of Q2 the voltage comparator (composed of Q2, Q3, and Q4) will turn on the switching transistor Q8. The LC filter action of choke L1 and comparator C7 smoothes the pulse waveform (see Figure 5-4). The voltage capacitor has a small amount of hysteresis (about 80 mv) so that the output voltage must increase to 5.04v before Q8 will be turned off, and must decrease to 4.96v before Q8 will be turned on again.

5.2.1.2 Overcurrent Protection

Current to the load is sensed across R22 by Q9. The values of R20 and R23 are selected such that Q9 will turn on when the current to the load exceeds 9 amps. The conduction of Q9 causes SCR1 to fire, which removes the base drive from Q6, turning Q8 off.

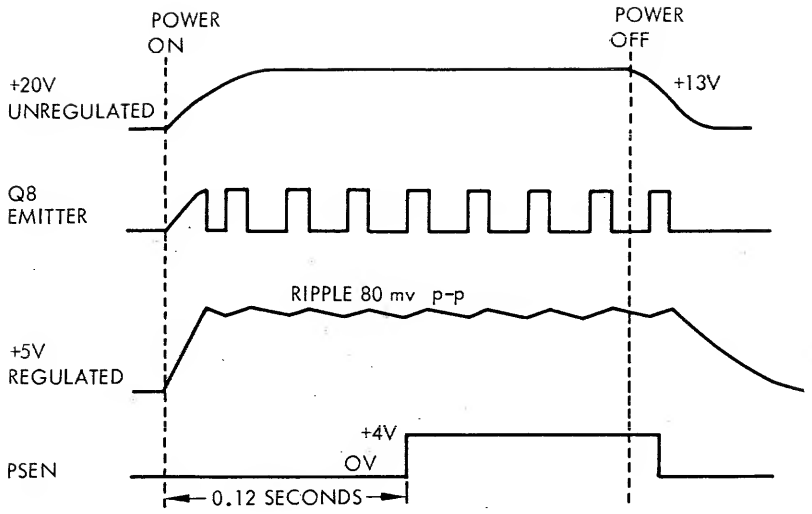


Figure 5-4. Switching Regulator Waveforms

It is important to note that the supply will not restart automatically when the overload condition is removed. It is necessary to turn off ac power for approximately 1 minute before turning power on again. This is the time required for C2 and C3 to discharge and remove the holding current from SCR1.

5.2.1.3 Overvoltage Protection

If the output voltage to the load exceeds 7.5v the supply fuse F2 will open removing the unregulated +20v supply from the regulator. A zener diode, CR13, generates a voltage 6.8v lower than the output voltage at the gate of SCR2. If the output voltage exceeds 7.5v SCR2 is turned on, causing fuse F2 to open. When the reason for the overvoltage has been corrected the fuse must be replaced.

5.2.1.4 Logic Enable (PSEN)

The logic enable signal, PSEN, is used to reset all formatter logic to the quiescent state. This is done while the +5v supply is being established after power is applied, and while the supply is decaying after power turns off. This ensures that the logic is in a defined state after power on, and that no spurious signals are sent to the transport logic.

When ac power is applied, the regulated output builds up to +5v causing C11 to charge through R24 and R27. When the voltage on C11 reaches 2.5v the voltage on the base of Q10 will be greater than the +3v on the base of Q11. Q10 and Q12 will then turn on causing the output PSEN to go to +4v approximately 0.12 second after power is applied.

A loss of ac power is detected by Q10 when the voltage on C8 and C9 drops below +13v. This occurs after the absence of one-half cycle of ac power and causes Q12 to turn off and the PSEN output to go to 0v, resetting the formatter logic.

5.3 FIXED OSCILLATOR

A fixed frequency oscillator subassembly is used on the NRZI PCBA and the PE Write/Control PCBA. This oscillator consists of an etched board approximately 2.5 inches square which is attached to the PCBA by four nylon standoffs. Interconnections between the oscillator and PCBA are made by a flat cable and a 14-pin IC connector which mates with J4 on the PCBA. The subassembly can be easily removed for repair or replacement.

The oscillator generates a fixed frequency clock that controls all basic timing within the formatter. The frequency of the oscillator is controlled by a 10-turn potentiometer and is adjusted according to tape speed. For the NRZI PCBA, the oscillator is set to 18 times the data rate at 800 cpi; for the PE Write/Control PCBA it is set to 6 times the data rate at 1600 cpi, e.g.,

NRZI	PE
$f = 18 \times 800 \times S \times 10^{-3}$	$f = 6 \times 1600 \times S \times 10^{-3}$
$= 14.4S$	$= 9.6S$

where

f = frequency in kHz
S = tape speed in ips

For a tape speed of 37.5 ips

$f = 14.4 \times 37.5 = 540$ kHz, for NRZI PCBA

and $f = 9.6 \times 37.5 = 360$ kHz, for PE Write/Control PCBA

There are three different fixed oscillator assemblies. The one installed on a particular formatter depends on the type of application and the date of shipment. Schematics and assembly drawings relevant to the companion formatter are included in this manual. Reference should be made to the schematic and assembly drawings for the following discussion.

(1) Single Speed Fixed Oscillator
Assembly 101362
Schematic 101361

(2) Single Speed Fixed Oscillator
Assembly 102096
Schematic 102095

(3) Dual Speed Fixed Oscillator
Assembly 101995
Schematic 101994

The two single speed oscillators are identical except that they use different etched board assemblies. They are directly interchangeable and are used when all transports attached to the formatter are of the same speed.

The dual speed oscillator consists of two independent oscillator circuits, and is used when transports of two different tape speeds are attached to the formatter. The condition of the transport configuration line, ISPEED, selects one oscillator circuit or the other.

Each oscillator assembly is versioned to cover tape speeds in the range of 6.25 to 75 ips.

The basic oscillator circuit is similar for all three assemblies. It consists of an emitter-coupled multivibrator circuit composed of transistors Q1 and Q2. Operating frequency of the circuit is determined by components

C2, R5, and potentiometer R4. Typical waveforms for this circuit are shown in Figure 5-5. The waveform appearing at the emitter of Q2 is amplified and inverted by Q3 to form the output clock waveform.

The dual speed oscillator, Assembly 101995, contains a second oscillator circuit composed of Q5, Q6, and adjustment potentiometer R17. The outputs of the two oscillators are ORed together at the base of Q3.

The incoming control waveform, SPEED, disables one oscillator or the other by opening the emitter return of Q2 or Q6. The SPEED line is high-true at this point; hence oscillator Q1, Q2 corresponds to the higher tape speed (and frequency), and oscillator Q6, Q7 corresponds to the lower tape speed (and frequency).

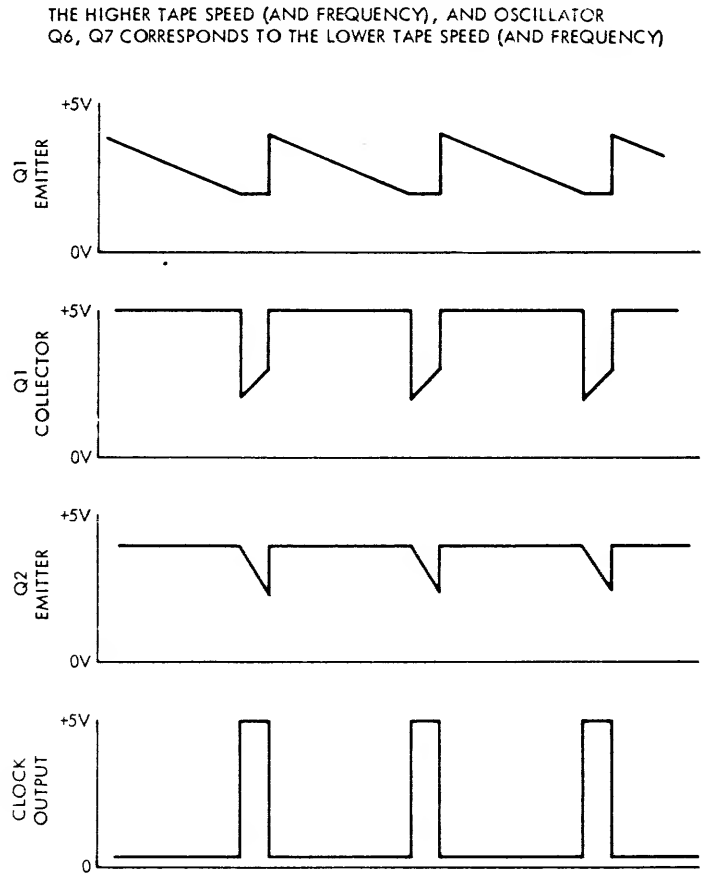


Figure 5-5. Fixed Oscillator Waveforms

5.4 TRACKING OSCILLATOR

A tracking oscillator subassembly is used on the PE Read Recovery PCBA. This oscillator consists of an etched board approximately 2.5 inches square which is attached to the PCBA by four nylon standoffs. Interconnections between the oscillator and PCBA are made by a flat cable and a 14-pin IC connector which mates with J4 on the PCBA. The subassembly can be easily removed for repair or replacement.

The tracking oscillator controls all timing on the Read Recovery PCBA. It operates in conjunction with control logic on the Read Recovery PCBA, and generates a clock waveform whose frequency is always 24-1/2 times the instantaneous data rate of the phase mode read signals. In effect, the oscillator tracks tape speed and allows the read logic to compensate for average and instantaneous speed variations of the transport reading the tape.

When read signals are absent, the oscillator reverts to its center frequency at approximately the center of the tracking range. The center frequency, fc, is controlled by a 10-turn potentiometer, and is initially adjusted according to the nominal tape speed, as follows.

$$fc = 24\text{-}1/2 \times 1600 \times S \times 10^{-3}$$
$$= 39.2S$$

where

fc = center frequency in kHz
S = tape speed in ips.

For example, at a tape speed of 37.5 ips

$$fc = 39.2 \times 37.5$$
$$= 1470 \text{ kHz}$$

There are three different tracking oscillator assemblies. The one used in a particular formatter depends on the type of application and date of shipment. Schematic and assembly drawings relevant to the companion formatter are included in this manual. Reference should be made to the schematic and assembly drawings for the following discussions.

(1) Single Speed Tracking Oscillator
Assembly 101395
Schematic 101396

(2) Single Speed Tracking Oscillator
Assembly 102094
Schematic 102093

(3) Dual Speed Tracking Oscillator
Assembly 101990
Schematic 101989

The two single speed oscillators are similar, the difference being the use of different etched board assemblies. They are directly interchangeable and are used when all transports attached to the formatter are of the same speed.

The dual speed oscillator consists of two independent tracking oscillator circuits, and is used when transports of two different tape speeds are attached to the formatter. The condition of the transport configuration line, ISPEED, selects one oscillator circuit or the other.

Each oscillator assembly is versioned to cover tape speeds in the range of 6.25 to 75 ips.

The circuit used is essentially the same for the three assemblies. The following discussion refers specifically to Assembly 102094 and Assembly 101990.

The basic oscillator is an emitter-coupled multivibrator circuit consisting of transistors Q1 and Q2. Frequency is determined by components C2, R4, and potentiometer R5, and also by the dc tracking voltage applied to the base of Q1. The waveform appearing at the emitter of Q2 is amplified and inverted by Q3 to form the output clock waveform. Typical multivibrator waveforms are shown in Figure 5-6.

The tracking voltage, V_T, is varied by charging or discharging capacitors C1 and C5 under the control of two external waveforms, NER1 and NER2. The control waveforms are generated on the Read Recovery PCBA, and are used to servo the oscillator frequency in such a manner that there are more than twenty-four, and less than twenty-five, output clock pulses for each phase mode data cell. The oscillator frequency will therefore average twenty-four-and-one-half times the instantaneous data rate.

When NER1 is at 0v, capacitors C1 and C5 begin to discharge through R11 causing the oscillator frequency to decrease. When NER2 is at 0v, C2 and C5 begin to charge through R12 causing the oscillator frequency to increase.

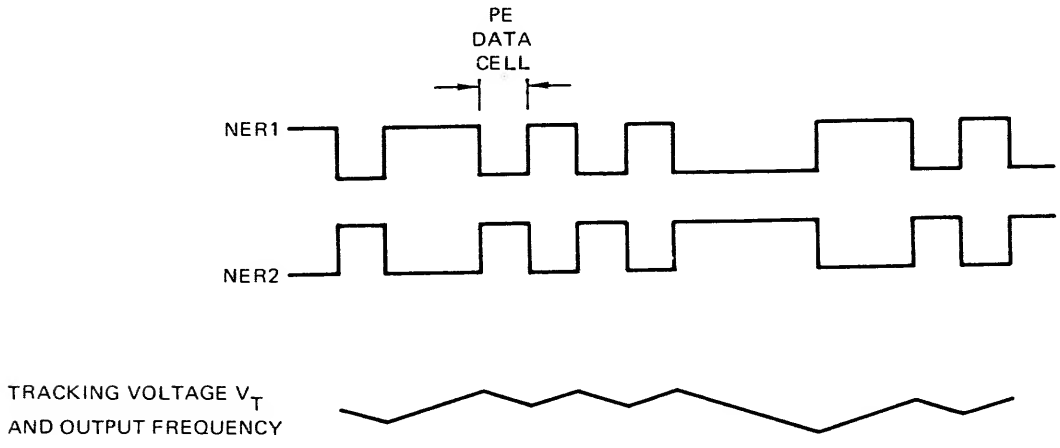


Figure 5-6. Tracking Oscillator Control Waveforms

The tracking range is defined by a voltage divider consisting of R1 and R2, and clamp diodes CR1 and CR2. R1 and R2 define a voltage of 1.6v, and the diodes limit excursions of V_T to within one diode drop of this figure. Hence,

$$V_T \text{ (max)} = 1.6 + 0.7 = 2.3v$$

$$V_T \text{ (min)} = 1.6 - 0.7 = 0.9v$$

This results in a tracking range of approximately ±25 percent above the center frequency.

When no data are being read, the formatter control logic holds both NER1 and NER2 to 0v. R11 and R12 now act as a voltage divider and define a voltage, V_T (center), that determines the oscillator center frequency. The ratio of R11 to R12 is chosen so that this is at approximately the center of the tracking range (~1.6v).

The maximum tracking rate is determined by components R11, C1, C5, when tracking upwards in frequency, and by R12, C1, C5, when tracking downwards in frequency. These rates are made equal, and are chosen to provide the best overall system tolerance for ISV amplitude, ISV frequency, and for differences in average tape speed. A tracking rate of approximately 10 percent in 35 character periods is used on all tracking oscillators. Typical operation of the tracking oscillator is shown in Figure 5-7.

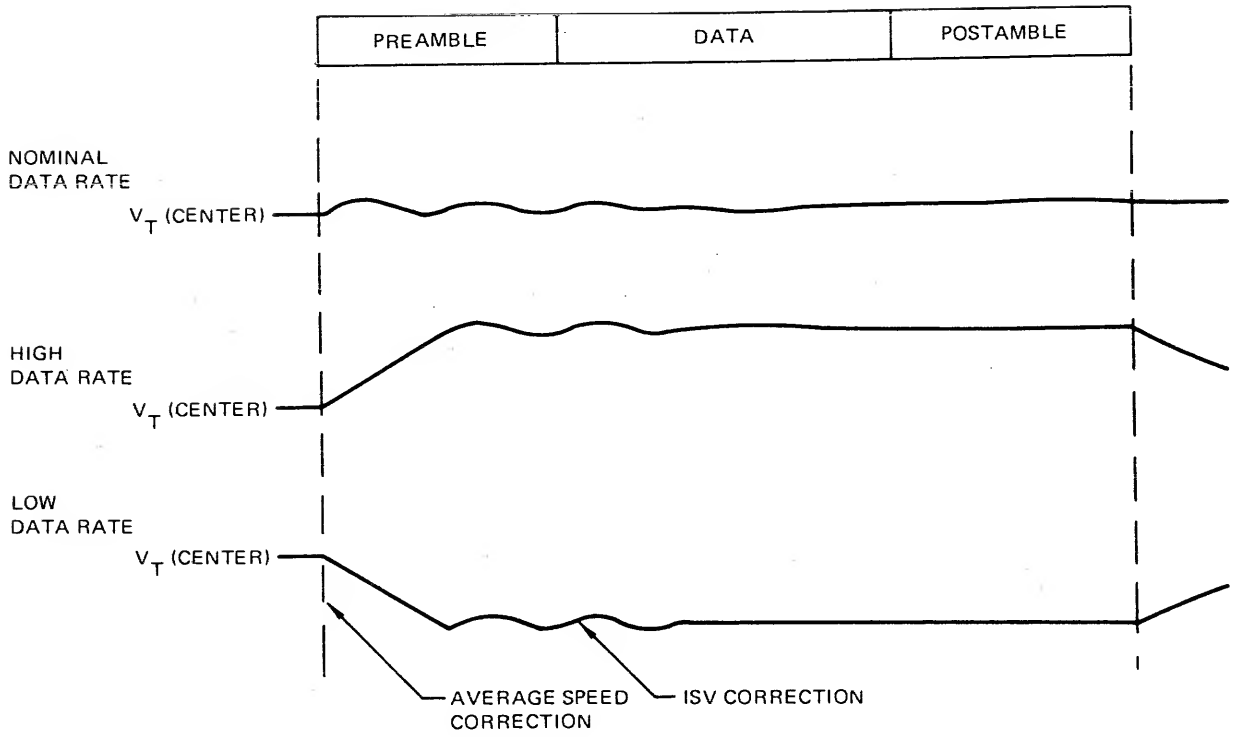


Figure 5-7. Operation of Tracking Oscillator

5.5 PE WRITE/CONTROL PCBA

The Write/Control PCBA is one of the two logic board assemblies employed in the PE Formatter. Refer to Schematic 101385 and Assembly 101386 for the following discussion.

The Write/Control board contains the logic used to write phase encoded data onto tape and provides the various control and timing functions required by the formatter. Another logic assembly, the Read Recovery PCBA, contains all logic associated with reading phase encoded data.

Both the Write/Control PCBA and the Read Recovery PCBA are employed in formatters having full read/write capability. For a Read Only formatter, both PCBAs are used but the write logic is omitted from the Write/Control PCBA. For a Write Only formatter, only the Write/Control PCBA is required.

The Write/Control PCBA performs the following major logic functions.

(1) Formatter and transport address selection.

(2) Status and configuration reporting of the selected transport to the controller.

(3) Interpretation and storage of various formatter commands.

(4) Provides the basic control and timing required for the execution of commands including the interchange of control signals with the Read Recovery PCBA.

(5) Write control logic.

(6) Encodes write data, preamble, and postamble patterns into phase encoded form for transmission to the transport.

Schematic 101385 (sheet 1 of 6) illustrates the physical layout of the PE Write/Control PCBA. Interconnections to the controller and transport interfaces are made through two 100-pin edge connectors, J1 and J2, respectively. J1 also carries local control signals between the Write/Control PCBA and the Read Recovery PCBA. It is important to note that pin connections at J1 and J2 are reversed at the external formatter interface connectors. For example, a signal on J1-A3 appears on J101-B3 or J103-B3 at the external connectors. Sheet 2 of 6 of Schematic 101385 provides identification of the signals present at J1 and J2 as referenced in the text.

Ground and +5v power connections are made through J1 and J2 in parallel. Pins B48, B49, and B50 supply the +5v, and pins A48, A49, and A50 are used for ground. The PCBA draws approximately 2-1/4 amps from the +5v supply.

A removable fixed oscillator assembly is mounted at the front left of the PCBA and mates with a 14-pin IC connector, J4. The oscillator generates a clock waveform which controls the timing of all PCBA waveforms.

Selection of the internal/external Write parity option is made on a jumper platform assembly which mates with the IC connector, J6. Other jumpers on this platform are used to ground the transport configuration lines as required when the formatter is dedicated to a particular transport type.

Four different versions of the Write/Control PCBA, Assembly 101386, are required to cover the various formatter applications.

(1) Assembly 101386-01 — Standard version. This version consists of a PCBA with a full complement of ICs and is used in single, Read/Write, and Write Only formatters.

(2) Assembly 101386-02 — Controller interface terminators omitted. This version is used in dual PE/NRZI formatters which have separate transport interface ports.

(3) Assembly 101386-03 — Controller and Transport interface terminators omitted. This version is used in dual PE/NRZI formatters having a common transport interface port.

(4) Assembly 101386-04 — Write logic omitted. This version is used for single Read Only formatters. In this version two other jumpers, W1 and W2, are added to the PCBA. These jumpers provide grounds for signal lines that would otherwise be floating.

5.5.1 FORMATTER AND TRANSPORT ADDRESS SELECTION, CIRCUIT DESCRIPTION

The formatter address is pre-selected by a 3-position switch, S1 (sheet 3 of 6, zone H7) on the Write/Control PCBA. The first switch position is an "off" position in which the formatter will not recognize any address. The second and third positions correspond to an address of "0" and "1", and are wired to the appropriate polarity of the formatter address line, IFAD.

When the address specified by the controller agrees with the switch setting, the switch output FSLT (formatter selected) goes high and the formatter is connected to the controller. FSLT, and its inverse NFSLT, are routed to various parts of the logic to perform the required gating.

When selected, the formatter routes the transport address lines ITAD0 and ITAD1 (sheet 3 of 6, zone G8) to four gated driver elements. These drivers decode the individual transport select lines, ISLT0-3, as follows.

ITAD0	ITAD1	Select Line
0	0	ISLT0
0	1	ISLT1
1	0	ISLT2
1	1	ISLT3

By virtue of the coding, only one of the four select lines can be true at a time. When the formatter is not selected, transport 0 (ISLT0) is always selected.

Another input to the drivers, PSEN (power supply enable) (sheet 3 of 6, zone G8), causes all select lines to be disabled when power is applied or removed from the formatter. This prevents the transports from responding to spurious signals which might occur on other interface lines during this period. Resistor R74 provides a load for the transistor that generates PSEN. Additionally, it serves as a ground to disable the formatter in the case of a broken cable.

5.5.2 TRANSPORT STATUS AND CONFIGURATION LINES, CIRCUIT DESCRIPTION

Status and configuration information from the selected transport is reported to the formatter on the following lines.

(1) STATUS: IRDY, IONL, IRWD, IFPT, ILDP, IEOT.

(2) CONFIGURATION: INRZ, ISGL, ISPEED

The three configuration lines (sheet 3 of 6, zone C6) are provided with ground jumpers at J6 which allow the formatter to be dedicated to a particular transport type.

Each of the status and configuration lines is gated with NFSLT (formatter selected) (sheet 3 of 6, zone H6) then retransmitted through a driver element to the controller interface. When necessary, the inverse waveform is generated for internal formatter use.

5.5.3 RESET (RST)

A general reset waveform, RST, is formed by the 4-input gate, A8/8 (sheet 3 of 6, zone E7). When true, this signal causes all control logic in the formatter to be dc reset to the inactive state. This reset occurs if any one or more of the gate inputs is low, as follows.

(1) FSLT – when the formatter is not selected.

(2) NNRZ – the selected transport is not phase mode.

(3) PSEN – power is being applied to or removed from the formatter.

(4) FEN – the formatter is being reset by the controller.

Capacitor C26 provides filtering of high-frequency noise transients (less than 500 nanoseconds) which could be picked up at the interface on IFAD, IFEN, and INRZ when the system is operated in a heavy noise environment.

5.5.4 CLOCK LOGIC

Included on the Write/Control PCBA is a fixed oscillator assembly which generates a clock waveform that controls all timing on the PCBA. The frequency is set to 6 times the phase mode data rate at 1600 cpi.

$$f = 6 \times 1600 \times 10^{-3} \times S$$
$$= 14.4S$$

where

f = frequency in kHz

S = tape speed in ips

A description of the various fixed oscillator assemblies (single and dual speed) and the relevant schematic and assembly identification number is contained in Paragraph 5.3.

The oscillator output, CLKS, is applied to a 3-stage counter that divides the input by six. The first two stages, CCTR0 and CCTR1, divide by three, and the third stage toggles CCTR1 for a further divide by 2.

Typical waveforms are illustrated in Figure 5-8. The falling edge of ODD marks the boundary between adjacent phase mode data cells. Waveform ODD is true during the odd half of each bit cell, and the inverse, NODD, is true during the even half.

CCTR1 and ODD are gated together at B8/8 (sheet 4 of 6, zone D2) and the result is re-inverted to form CCLK (character clock). CCLK is used to clock all timing and control flip-flops on the PCBA.

Another waveform, WCLK (write clock) (sheet 4 of 6, zone C1) is generated in a similar manner by gating CLKS, NCCTR0, CCTR1, and WCN6. The first three inputs define a pulse at the end of each half cell period, and the fourth, WCN6, enables the output during certain parts of a Write command. This waveform clocks the register which encodes write data into phase mode form.

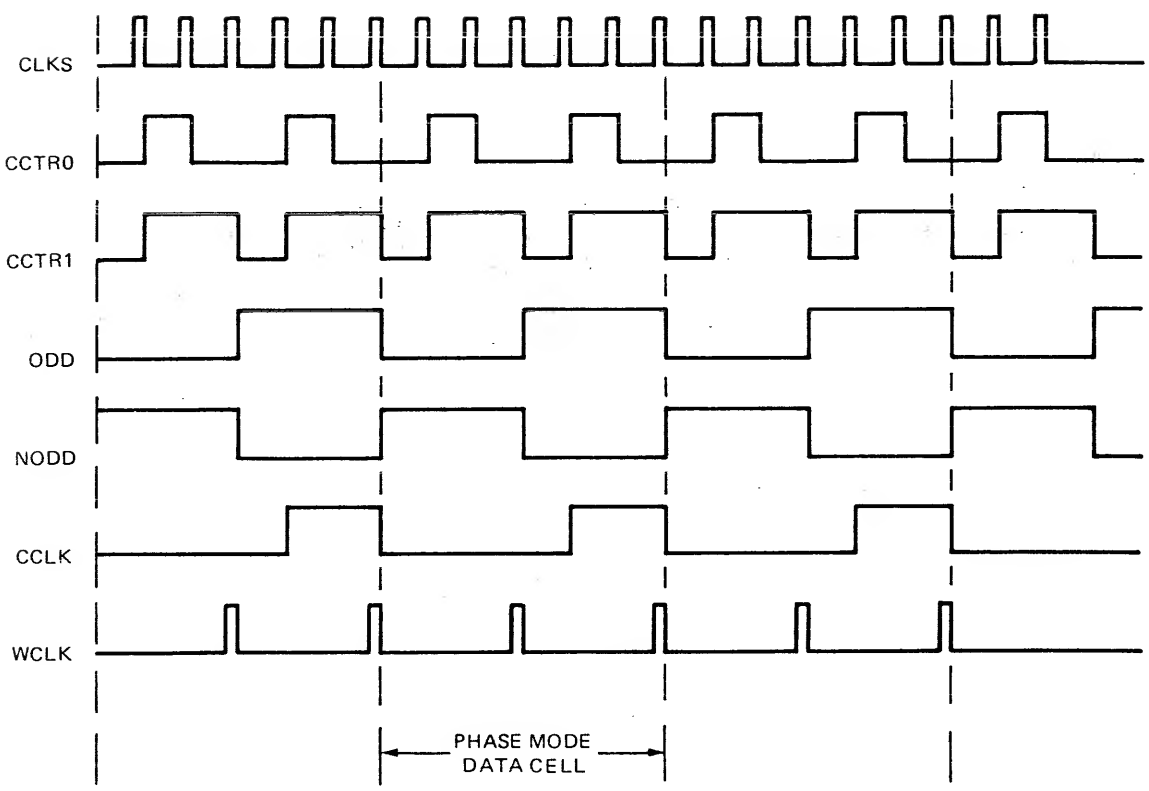


Figure 5-8. Clock Waveforms

5.5.5 FORMATTER COMMANDS

The Rewind (IREW) and Off-line (IOFL) commands differ from other formatter commands in that they are obeyed by the transport logic and do not cause the formatter to go busy. The IREW and IOFL lines (sheet 3 of 6, zone F8) are gated with NFSLT and retransmitted to the transport interface on IRWC and IOFC, respectively.

The controller initiates other commands by setting a group of coded command lines to the required state and pulsing IGO. Coding for the various commands is shown in Table 3-1.

IGO (sheet 4 of 6, zone G8) is gated with DCN5 (formatter ready for new command) and RDY (selected transport ready), then inverted to form the GOP (GO pulse). GOP is a high-true pulse that is connected to the clock inputs of a 7-stage command register (sheet 3 of 6, zone H2). On the falling edge of GOP each command line is copied into a corresponding register stage. The command remains stored in the register until it is either overwritten by the next command, or the register is dc reset by NRST.

Outputs from the command register control the various formatter operations, and in some cases serve as control signals to the transport interface (ISWS, IREV, IOVW, IRTH1, and IRTH2).

Initial synchronization with CCLK is performed by flip-flops GO1, GO2 (sheet 4 of 6, zone H6) and DCN5. Typical waveforms are shown in Figure 5-9. GO1 is clocked true by the falling edge of GOP and causes GO2 to set on the trailing edge of the next CCLK pulse. One clock time later, DCN5 sets and GO2 is reset via the K input. DCN5 now dc resets GO1 and disables GOP, preventing the formatter from recognizing any further commands until the current command is completed. Thus, GO2 consists of a single pulse, one clock period wide at the beginning of each formatter command.

5.5.5.1 Delay Logic

All commands (except Rewind and Off-line) are executed in the following manner.

(1) A pre-record delay is generated during which time the tape ramps up to speed and traverses the IBG.

(2) Data transfer now takes place under the control of the read and/or write logic.

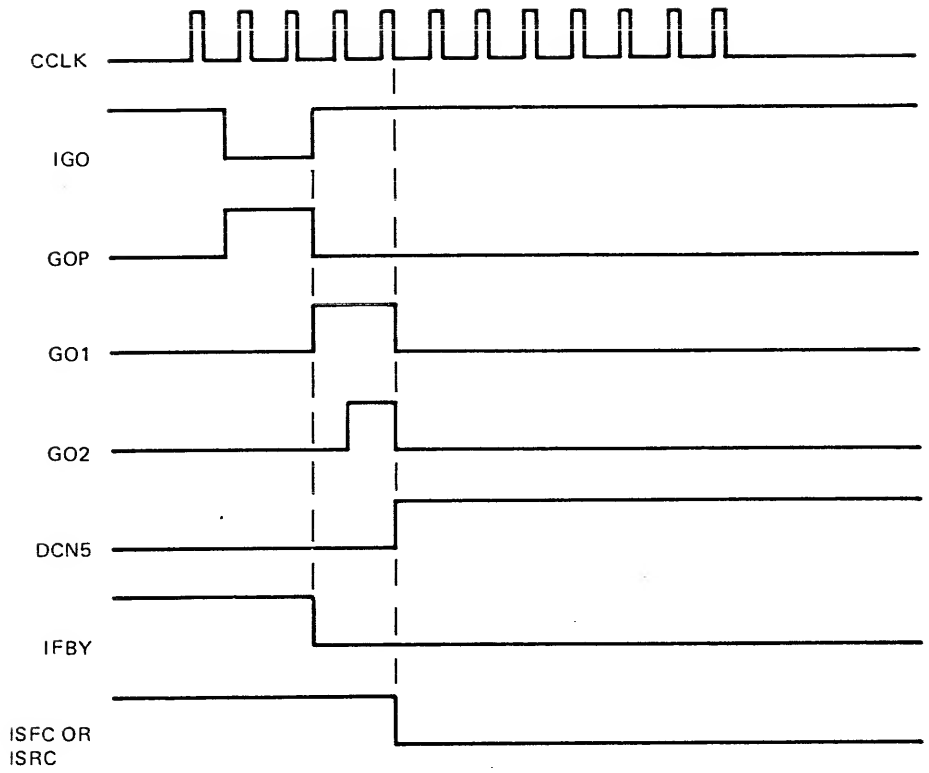


Figure 5-9. Command Initiation Waveforms

(3) On completion of the command, a post-record delay is generated which determines head positioning in the IBG after the record.

(4) Finally, a rampdown delay is generated during which the tape decelerates to rest.

Different pre-record and post-record delays are required for the various formatter commands. All delays are scaled to the required tape speed by selecting the appropriate oscillator frequency. Table 5-1 lists these delays and shows specific values at a number of common tape speeds.

Table 5-1

Formatter Delays

	Delay	Control Flip-Flop	Gate	Tape Speed (ips)						
				6.25	12.5	18.75	25	37.5	45	75
Pre-Record Delays (msec)	Read from BOT	DCN1	C6/8	255.6	127.8	85.2	63.9	42.6	35.5	21.3
	Write from BOT	DCN1	C6/6	1023.6	511.8	341.2	255.9	170.6	142.2	85.3
	Read Fwd or Rev	DCN2	D7/6	51.0	25.5	17.0	12.7	8.5	7.08	4.25
	Write (Single Stack)	DCN2	D6/8	89.4	44.7	29.8	22.3	14.9	12.4	7.45
	Write (Dual Stack)	DCN2	D6/6	67.2	33.6	22.4	16.8	11.2	9.33	5.6
	Write File Mark	DCN2	D7/8	614.4	307.2	204.8	153.6	102.4	85.3	51.2
Post-Record Delays (msec)	Read Fwd	DCN3	C5/6	0.3	0.15	0.1	0.075	0.05	0.042	0.025
	Read Rev	DCN3	D5/6	12.6	6.3	4.2	3.15	2.1	1.75	1.05
	Read Rev (Edit)	DCN3	D5/8	22.2	11.1	7.4	5.55	3.7	3.08	1.85
	All Write Commands	DCN3	C5/8	12.6	6.3	4.2	3.15	2.1	1.75	1.05
	Rampdown Delay (ms)	DCN4	D4/6	76.8	38.4	25.6	19.2	12.8	10.67	6.4

Phase Mode Data Rate (kHz)	10	20	30	40	60	72	120
Fixed Oscillator Frequency (kHz)	60	120	180	240	360	432	720
Transport Start/Stop Ramp (msec)	60	30	20	15	10	8.3	5

The delays are generated by a counter circuit consisting of four control flip-flops (DCN1-4) (sheet 4 of 6, zone F3-6), a 16-bit ripple counter (DCTR1-16 (sheet 4 of 6, zone A3-7), a number of decoding gates, and associated logic. DCN1 is used for generation of the long pre-record delays associated with reading or writing from BOT, and DCN2 for the normal pre-record delays. DCN3 and DCN4 control the post-record and rampdown delays, respectively.

The gates decode counts equivalent to the various delays and are selected by suitable inputs from the control flip-flops and command register. Only one gate can be enabled at a time. The gate outputs are ORed together then connected to the J input of flip-flop DP (sheet 4 of 6, zone C4).

The ripple counter is initially clamped to the reset state by a false signal on DCNT (sheet 4 of 6, zone B3). When one of the control flip-flops is set, the 4-input gate C8/6 (sheet 4 of 6, zone B3) goes true and sets DCNT. The counter is now enabled and proceeds to count CCLK pulses (one every PE data cell) until the required delay has been accomplished.

When the required count is reached, the selected gate operates and a pulse is generated on DP during the following clock time. The counter is immediately reset by NDP on C3/1 (sheet 4 of 6, zone A8) and the control flip-flop is reset at the end of the same clock time. DCNT now goes false, re-applying the clamp to the counter, and the delay cycle is completed.

The counter circuit is also used to generate the 40-bit preamble and postamble patterns required during write operations. Control waveform (WCN1+5) (sheet 4 of 5, zone C4) and decoding gate D4/8 are used in this case.

5.5.6 COMMAND EXECUTION, CIRCUIT DESCRIPTION

Refer to Figure 5-10 in conjunction with Schematic 101385 for the following description. Upon receipt of a command, NGO2 causes either DCN1 or DCN2 to set, depending on whether or not the tape is at Load Point. The pre-record delay is then generated as described in Paragraph 5.5.3.1. The DP pulse for this delay is gated through B5/8 (sheet 4 of 6, zone F4), E8/4, and B6/4, to form the waveforms SP and SWP. SP consists of a pulse at DP time which marks the end of the pre-record delay for all commands. SWP is a similar waveform for write commands only.

At this time either the Read Recovery PCBA is enabled by IRGATE, or the write logic is enabled by SWP, and the required data transfer takes place. When operating with a transport utilizing a dual stack head, both the read and write logic are enabled simultaneously, and a read-after-write data check takes place.

The end of data transfer is signalled by a pulse on REND (read end) or WEND (write end) from the read or write control logic. The combination AND/OR GATE B5/6 (sheet 4 of 6, zone G4) selects one or the other of these signals to initiate the post-record delay, as follows.

(1) WEND
   (a) Single Stack. All write commands.
   (b) Dual Stack. Erase commands only.

(2) REND
   (a) Single Stack. All read commands.
   (b) Dual Stack. All read and write commands, except erase.

During a read-after-write operation, the waveform NWCN7 at B5/3 (sheet 4 of 6, zone G4) inhibits any spurious REND pulse that could occur (because of tape dropouts, etc.) until the complete record has been written.

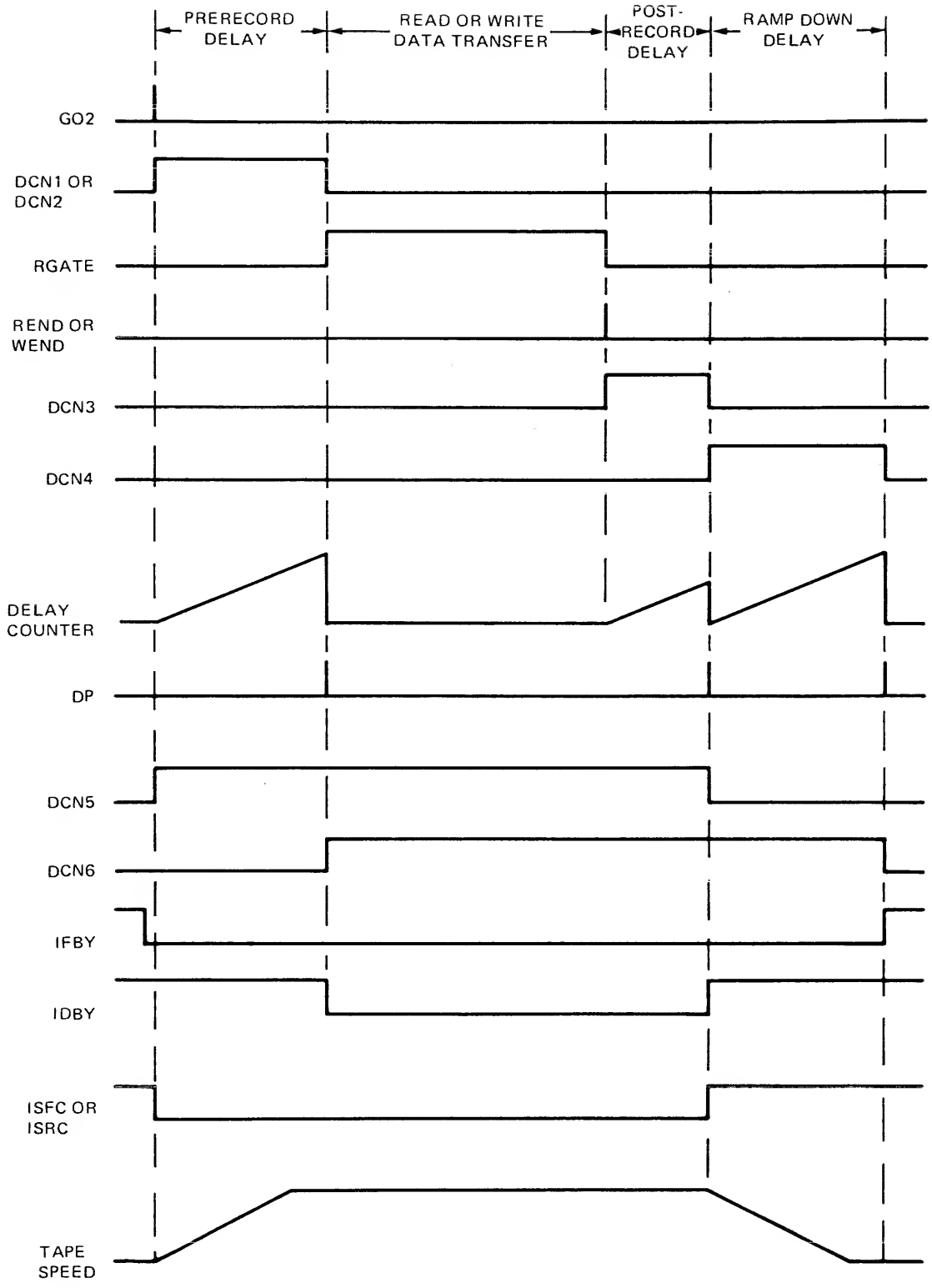


Figure 5-10. Command Timing

B5/6 now sets DCN3 via the present input, and the appropriate post-record delay is generated. At the end of this delay DCN3 and the counter are reset, and DCN4 is set by B6/13 (sheet 4 of 6, zone F3). The ramp-down delay is now generated during which the tape decelerates to rest. At the end of this period, execution of the current command has been completed, and the logic reverts to the idle state until the next command is received.

5.5.6.1 Control Waveforms

Flip-flops DCN5 (sheet 4 of 6, zone G4) and DCN6 assist in the generation of other formatter waveforms. DCN5 is set by GO2 at the beginning of a command, and reset at the end of the post-record delay. It represets the times during which tape motion is required. DCN6 is set at the end of the pre-record delay, and reset at the end of the rampdown delay.

The following waveforms are derived from DCN5 and DCN6.

(1) FBY (Formatter Busy) (sheet 4 of 6, zone G1). Formed by ORing GO1, DCN5, and DCN6 at B7/8. FBY goes true coincident with the trailing edge of GO and remains true until the command has been fully executed. The controller will normally make use of this waveform to inhibit further commands. It can also be used to verify that a command has been accepted by the formatter logic.

(2) DBY (Data Busy) (sheet 4 of 6, zone G1). DCN5 and DCN6 are gated at C7/13 to form this waveform. DBY goes true when the read or write data transfer begins, and resets when a stop command is given to the transport. The trailing edge of this waveform informs the controller that the transfer is complete, and that all errors have been reported.

(3) RGATE (Read Gate) (sheet 5 of 6, zone C1). This is the enable signal to the Read Recovery PCBA. RGATE is formed at E2/6 and D2/6 by gating DBY, NDCN3, and the output of C3/6. It is true from the end of the pre-record delay to the beginning of the post-record delay for all read commands (single or dual stack), and for write commands on a dual stack head (read-after-write).

(4) SFC and SRC (Tape Motion Commands) (sheet 3 of 6, zone H1). SFC and SRC are formed by gating DCN5 with the appropriate polarity of the Forward/Reverse command flip-flop at C7/10 and C7/4, respectively. SFC causes forward tape motion, and SRC causes reverse tape motion.

5.5.6.2 On-the-Fly Operation

The controller may issue a new command to the formatter during the rampdown delay (after DBY has gone false) provided that the new command is in the same read/write and forward/reverse status as the previous one. The controller must furnish the logic necessary to detect these conditions. This results in a time saving of up to one ramp time (the rampdown delay) per command. Figure 5-11 illustrates the waveforms encountered during an on-the-fly operation.

In this mode DCN4 (sheet 4 of 6, zone F3) and DCN6 are still set when the new command is issued. GO1 resets these flip-flops via OR gate B6/1 (sheet 4 of 6, zone E5) and the remainder of the rampdown delay is cancelled. At the same time DCNT goes false and the delay counter is reset. DCN1 now sets, and the pre-record delay for the new command is generated in the normal manner.

FBY is held true continuously during on-the-fly operation and resets only when the rampdown delay times out.

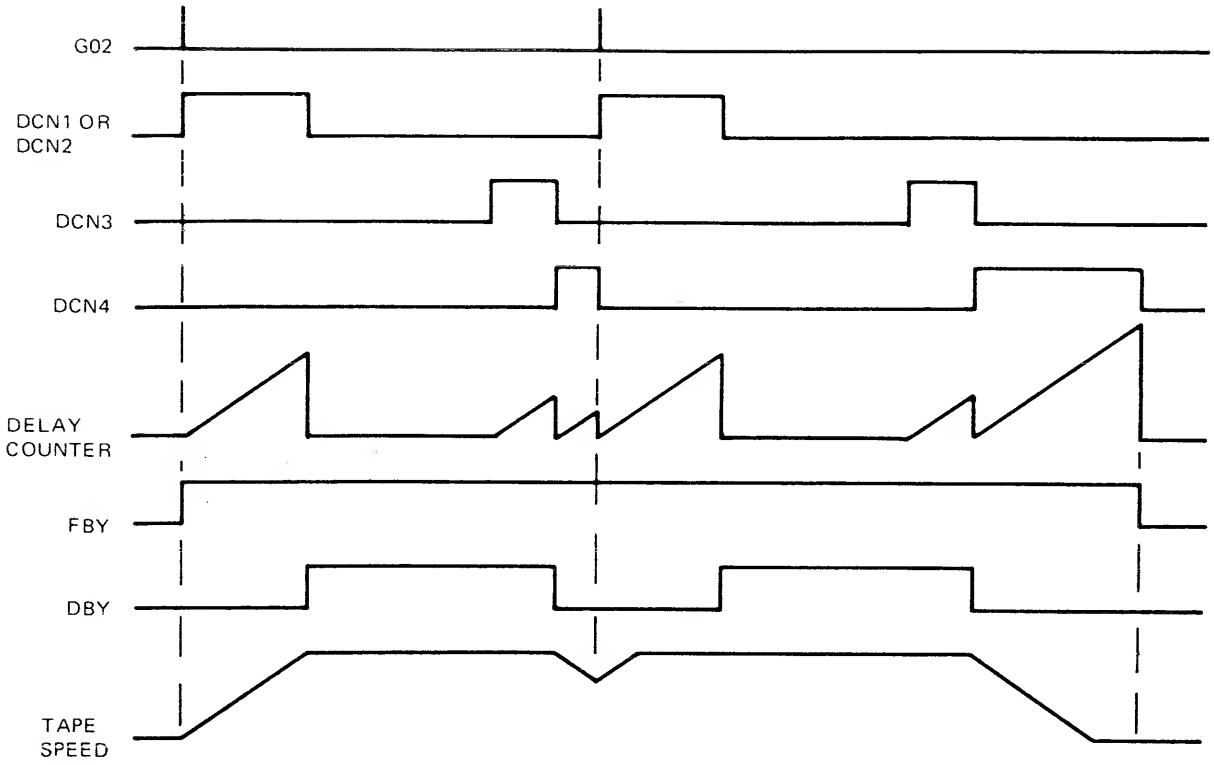


Figure 5-11. On-the-Fly Operation

5.5.6.3 Identification Timing

When writing from BOT, a PE identification burst is recorded on tape in the vicinity of the BOT tab. When reading from BOT, the read logic tests for the presence or absence of this burst and reports the result to the controller. These operations take place automatically during the pre-record delay and are closely associated with the delay counter timing.

Flip-flops ID (E3/15) (sheet 5 of 6, zone E3) and IDT (E3/11) are used to generate the identification waveforms. Figure 5-12 is a detailed timing diagram of the identification waveforms.

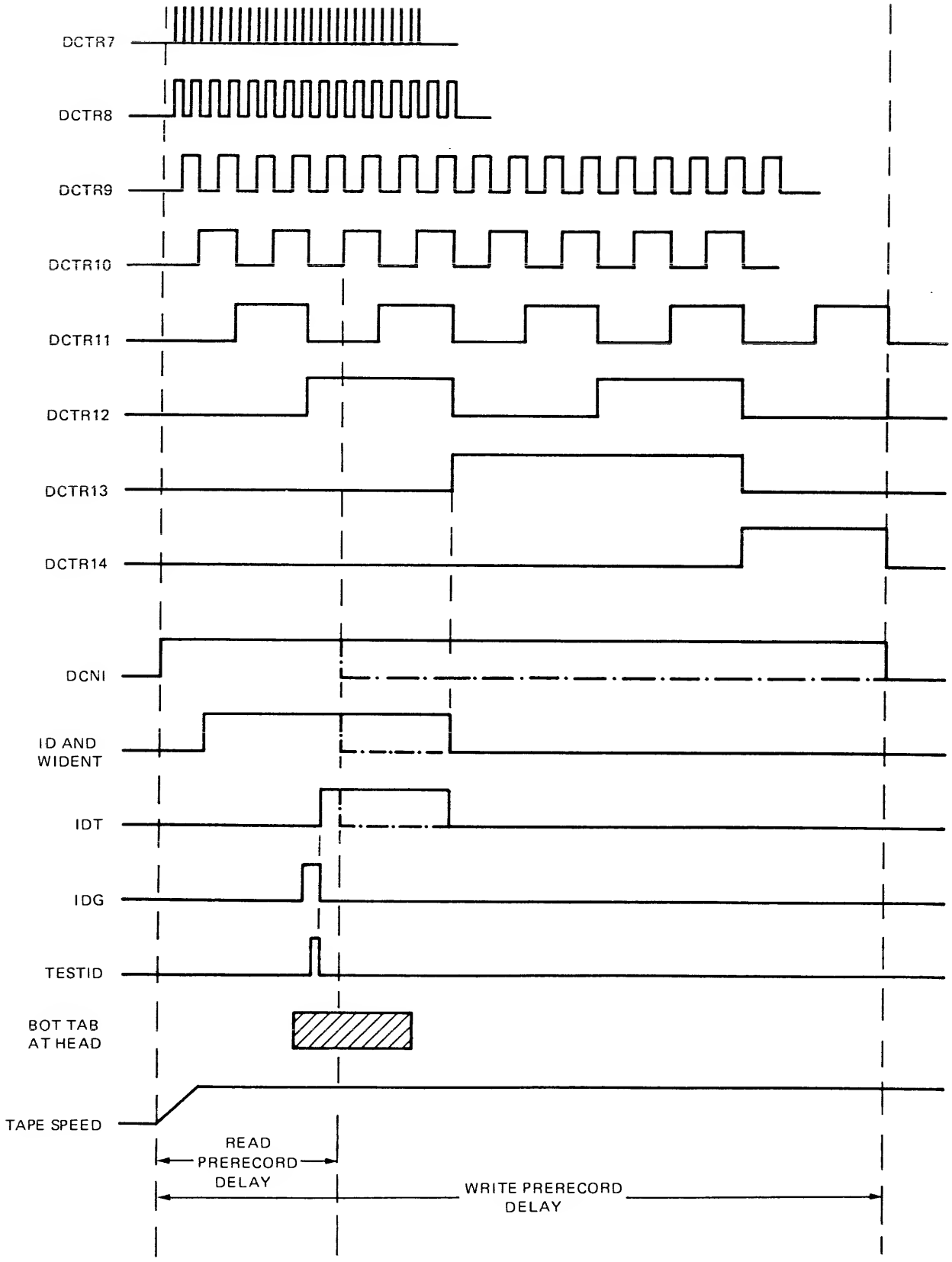


Figure 5-12. Identification Timing, Read and Write

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ID is initially clamped to the reset state by gates D3/13, C3/11, and E8/6. It is enabled when DCN1 is true, provided that DCTR13 and DCTR14 are both reset. A false signal on ID causes IDT to reset.

When a read or write command is issued at BOT, DCN1 goes true, ID is enabled, and the appropriate pre-record delay begins. ID is set true by the first falling edge on DCTR7 after DCTR10 goes true. This occurs shortly after the tape has reached operating speed. IDT is now enabled, and is set by the first falling edge on DCTR8 after DCTR12 goes true.

ID and IDT remain set until cleared at the following times.

(1) Read commands. When DCN1 resets at the end of the read pre-record delay.

(2) Write commands. When DCTR13 sets. During the remainder of the delay DCTR13 and DCTR14 inhibit further operation of the circuit.

A control signal, WIDENT, is formed by gating ID and WRT at D3/10 (sheet 5 of 6, zone D3). This signal goes true during write commands when the tape reaches operating speed, and remains true until the BOT tab moves past the read/write head stack. The PE identification burst is written onto tape during this time.

The Read Recovery PCBA requires two signals, IDG and TESTID, for the identification test. IDG (E2/8 and D2/8) (sheet 5 of 6, zone B2) is generated by gating ID, NIDT, and DCTR12, and goes true for a short time as the BOT tab moves over the read head. TESTID (D3/4, sheet 5 of 6, zone C2) is a gate of IDG and DCTR8 and is true during the latter half of IDG. IDG and TESTID are both disabled by C3/6 when writing on a dual stack transport.

IDG partially enables the read logic so that the presence or absence of identification data can be detected. TESTID performs the required test.

5.5.7 WRITE CONTROL LOGIC, CIRCUIT DESCRIPTION

The control and timing functions required during execution of write commands are performed by this logic.

Basic timing is achieved by two sets of flip-flops, WCN1-5 and WCN6-7 (sheet 5 of 6, zone G2-7). WCN1-5 set in turn and define the times during which the preamble, data, and postamble patterns are written. WCN6-7 form suitable gating waveforms for the generation of clock, strobe, and control patterns. The flip-flops have a common clock input, CCLK (one pulse each data cell), and are clamped to the reset state by DCN5 when not in use.

Figure 5-13 details the timing waveform of the write control logic. At the end of the pre-record delay, WCN1 is set true by SWP. (WCN1+5) goes high and the delay counter logic is enabled. The counter now counts 40 data cells which is the equivalent to the preamble zero bits. During the fortieth cell DP goes true causing WCN1 to reset, and WCN2 to set.

WCN2 remains true for one cell-time (preamble one bit), then WCN3 sets. During the following cell times write data from the controller is copied character-by-character into the write data logic. WSTR (sheet 5 of 6, zone B6) signals the controller when each character has been transferred.

When the last data character is transmitted the controller sets LWD (sheet 5 of 6, zone G7) true. At the end of this cell time WCN3 resets and WCN4 sets. WCN4 and WCN5 now time out the postamble one bit, and the 40 postamble zero bits, respectively.

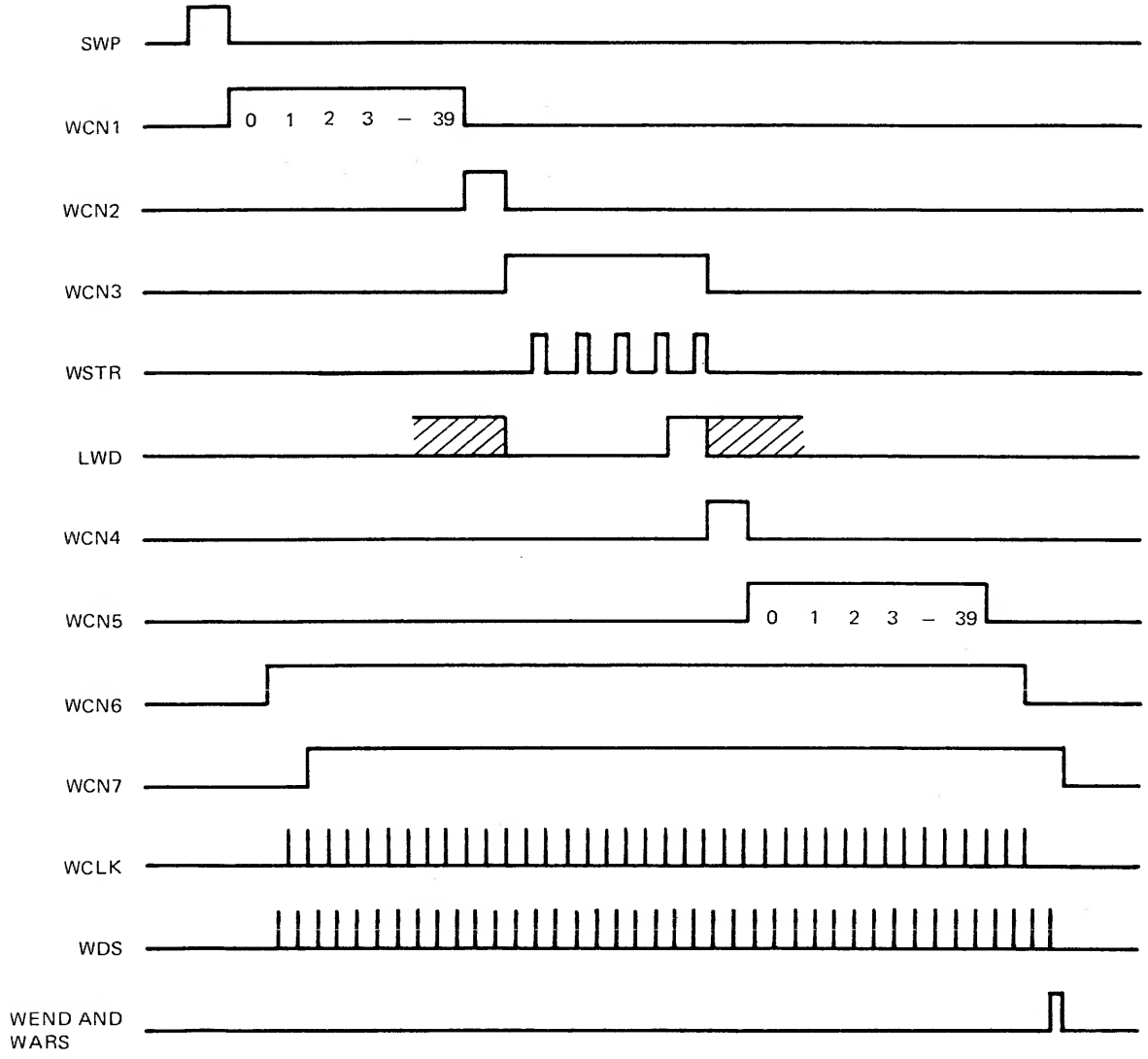


Figure 5-13. Write Sequence

During a WRITE FILE MARK command, WCN2-5 are clamped reset by the connection of WFM to H10/3 (sheet 5 of 6, zone F7). In this case only the 40-bit preamble pattern will be generated.

Note that WCN1-5 correspond to the times during which data is presented to the encoding logic. Each bit is encoded and recorded onto tape during the following cell time.

The input to WCN6 is formed by ORing together the times at which data patterns are recorded on tape. WCN1-5 are ORed at G8/8 (sheet 5 of 6, zone F4), then this is ORed with WIDENT, the time when the PE identification burst is to be written. The resulting waveform is delayed one cell time each by WCN6 and WCN7, to form the required gating waveforms.

In addition to the signals and waveforms previously discussed, the following interface waveforms are generated by the Write control logic.

(1) WSTR (sheet 5 of 6, zone B6). This signal controls the transfer of write data from the controller to the formatter. It is formed by gating CCLK and WCN3 at E13/1. The controller should set up the next character on, or within, a half-cell time after the trailing edge of each WSTR pulse.

(2) WDS (sheet 5 of 6, zone D6). This pulse is formed by H9/11, H11/4, and G12/1. It consists of a pulse at the center of each half cell period when either WCN6 or WCN7 is set. It is used to copy the 9 channels of phase encoded data into the tape transport logic. The connection of NERASE to H9/12 inhibits this waveform during erase commands.

(3) WARS (and WEND) (sheet 5 of 6, zone C6). This signal is formed by gating CCLK, WCN7, NWCN6, and NDCN1 at C8/8 and G12/4. It consists of a pulse at the end of

the write sequence just after the last postamble bit has been recorded. WEND is used to initiate the post-record delay. WARS is employed to turn off write current in the selected transport when a WRITE (Edit) command is performed.

NOTE

Presence of DCN1 on C8/12 prevents generation of a pulse when the identification burst is written.

The following are control waveforms which are generated by the Write control logic for the Write data logic of the formatter.

(1) WCLK (sheet 4 of 6, zone C1). This waveform is described in Paragraph 5.5.4.

(2) NWTOG (sheet 5 of 6, zone G1). This is formed by gating WCN6 and NODD at E11/6. It is low during the even (first) half of each bit cell when WCN6 is set.

(3) NWONES (sheet 5 of 6, zone F1). This is formed by H9/3, G8/6, and H8/2. WIDENT and DCTR1 are first gated at H9/3 to form the identification data pattern (0101). The output of H9/3 is then ORed with NWCN2, NWCN4, and NWTOG at G8/6. The result is inverted to form NWONES. This waveform is low during the even half cell if a zero bit (preamble, postamble, or identification) is to be recorded, or is low for the complete cell time if a one bit is to be recorded. Waveforms for NWTOG and NWONES are shown in Figure 5-14.

(4) NWRES1 (sheet 5 of 6, zone G1). This is the reset line for Channels 0, 2, 5, 6, and 7 of the encoding register. It is formed by gating WCN6 and NDCN1 at H9/6. These channels are enabled when WCN6 is set (data is being recorded onto tape), except during the pre-record delay.

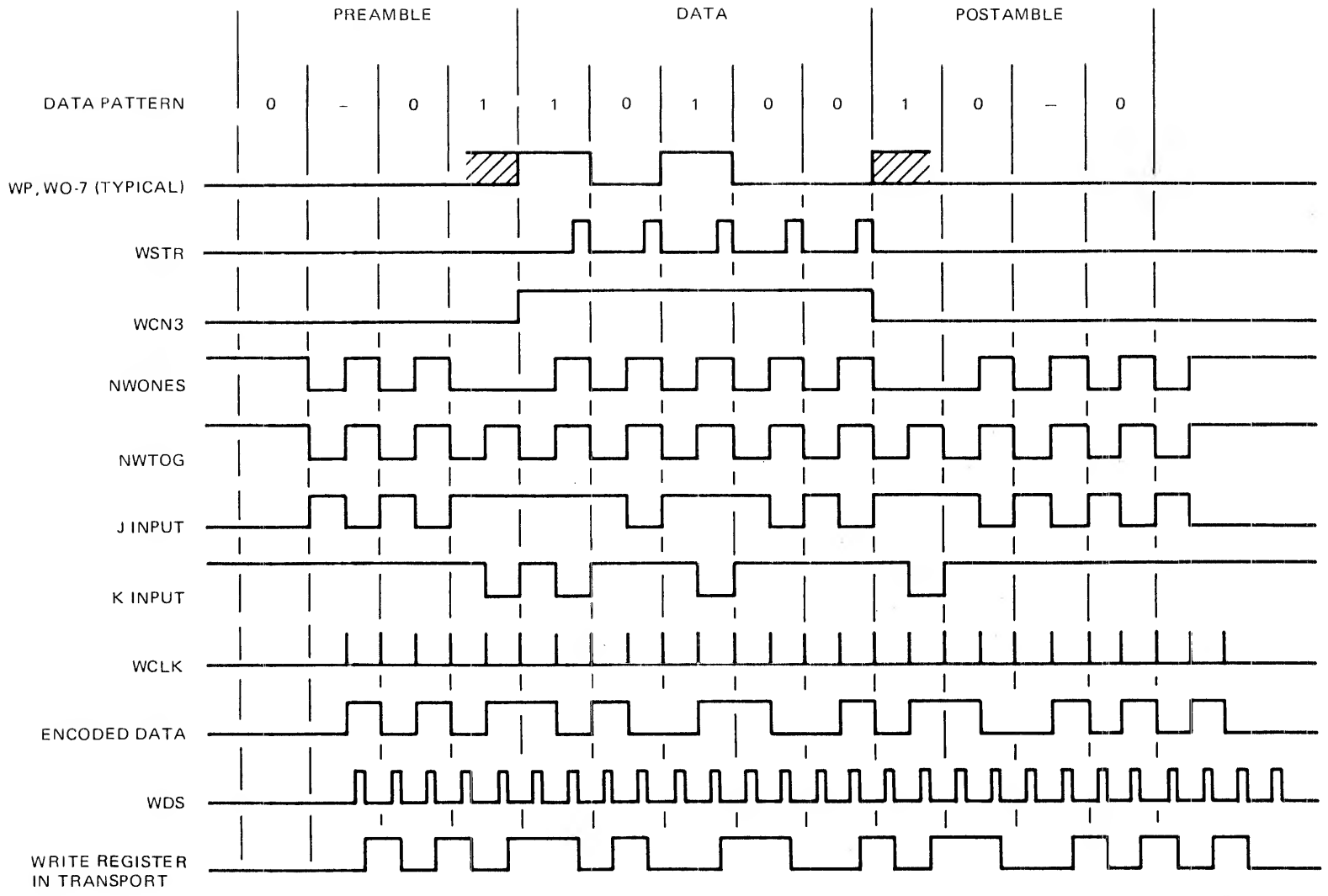


Figure 5-14. Write Data Encoding

(5) NWRES2 (sheet 5 of 6, zone F1). This is the reset line to Channels 1, 3, and 4 of the encoding register, and is formed by gating NWRES1 and WFM at H10/10. These channels are enabled when WCN6 is set, except during the pre-record delay or a WRITE FILE MARK command.

The sequence of events which occur during the execution of different write commands can be summarized as follows.

(1) WRITE (Normal) / WRITE (Edit). At the end of the pre-record delay, the preamble, data, and postamble patterns are generated and recorded onto tape. WEND (or REND for a dual-stack head) initiates the post-record delay, then a stop command is given to the transport. The head comes to rest further into the IBG for a write command than for a read command.

(2) WRITE From BOT. At the beginning of the pre-record delay WIDENT causes the PE identification burst to be written (see Figure 5-12). This consists of a 0101 pattern written only on Channel P, with the other channels erased. A read-after-write test for identification is also performed on transports utilizing a dual stack head. Approximately 3-1/2 inches of tape is then erased before the pre-record delay times out. The first data record is then written in the normal manner.

(3) WRITE FILE MARK. A long pre-record delay is generated (equivalent to a 3-1/2 inch gap), then a file mark pattern is recorded. This consists of 40 zero bits on Channels P, 0, 2, 5, 6, and 7, with the other channels erased.

(4) ERASE (Variable) / ERASE (Fixed). These commands are executed in the same manner as a WRITE or a WRITE FILE MARK command, respectively. In this case, WDS is inhibited and no data is copied into the transport electronics. The equivalent length of tape is erased.

5.5.8 WRITE DATA LOGIC, CIRCUIT DESCRIPTION

The incoming write data lines from the controller (IWP, IW0-7) (sheet 6 of 6, zone G8-B8) are terminated, then inverted to form WP, W0-7. W0-7 are fed to a parity generator which forms the odd parity bit, WPAR, for the eight data bits. Either WPAR, or the parity bit specified by the controller, WP, can be selected for writing on tape by suitable jumper connections on J6.

W0-7 and the selected parity are then fed to nine encoding circuits which add preamble, postamble, and identification information as required, and encode the result into phase mode form. The circuit for Channel 0 will be used as an example in the following description. Refer to Figure 5-14 for the appropriate waveforms.

Controller data (W0) is first gated with WCN4 at C11/8 (sheet 6 of 6, zone G5). The output of this gate goes low when a one bit is being transmitted. During the preamble, postamble, and identification times this gate is disabled (WCN3 false) and zero bits will normally be recorded onto tape.

Encoding is performed by two gates (D11/8 and D10/6) (sheet 6 of 6, zone F4), and a flip-flop (F10/15) which is clocked each half-cell time by WCLK when encoding is required. The encoding method is as follows.

(1) At the end of each cell the condition of the data bit to be recorded (0 or 1) is copied into the encoding flip-flop.

(2) A half-cell time later (center of the following cell) the flip-flop is toggled to the opposite state.

(3) At the end of this cell the next bit is copied, and the process is repeated.

The copy/toggle action is controlled by two waveforms, NWONES and NWTOG, from the write control logic (refer to Paragraph 5. 5. 5). During the odd half-cell these waveforms are normally high and the value of the data bit, and its inverse, are routed to the J and K inputs, respectively. One bits (for the preamble, postamble, and identification) are introduced by holding NWONES low during this time. This information is copied into the flip-flop by WCLK at the end of the half-cell period (at the cell boundary).

During the even half-cell, NWONES and NWTOG force the J and K inputs high, and the toggle action takes place.

When not in use, the nine encoding flip-flops are clamped to the reset state by WCN6, NWRES1, and NWRES2. When a data record is to be written, these signals go true and encoding takes place on all channels. For a WRITE FILE MARK command, NWRES2 remains low causing Channels 1, 3, and 4 to be erased. A file mark pattern (40 zeros) is encoded on the other channels. When writing identification, NWRES1 and NWRES2 are both low, and the identification pattern (0101) is encoded for Channel P only. The remaining channels are erased.

Encoded data for the 9 channels is routed through driver elements to the transport interface lines, IWDP, IWD0-7. This information is copied into a write register in the selected transport by WDS, then recorded onto tape.

5.6 PE READ RECOVERY PCBA

The Read Recovery PCBA is one of the two logic board assemblies employed in the PE Formatter. Refer to Schematic 101380 and Assembly 101381 for the following discussion.

The Read Recovery PCBA accepts phase encoded signals from tape in IBM format, converts this information into NRZI form, and transmits the result to the controller interface. Basic operations include the removal of preamble and postamble patterns, data decoding, deskewing, error detection, and error correction. The PCBA is designed for use with PERTEC 6600 and 7600 series of tape transports at tape speeds from 6.25 to 75 ips.

In most formatter applications this PCBA is used in conjunction with the PE Write PCBA (Assembly 101386). A number of internal control signals are interchanged between the two boards. In the case of a Dual Read-Only PE/NRZ Formatter the Write PCBA is not used, and control is provided by the NRZ PCBA.

Schematic 101380 (sheet 1 of 6) illustrates the physical layout of the Read Recovery PCBA. Interconnections to the Controller and Transport interfaces are made through two 100-pin connectors, J1 and J2, respectively. J1 also carries the internal control connections between the Write/Control (or NRZI) PCBAs. Note that pin connections at J1 and J2 are reversed at the external formatter interface connectors. For example, a signal on J1-A37 appears on J101-B37 or J103-B37 at the external interface. Sheet 2 of 6 of Schematic 101380 provides identification of the signals present at J1 and J2 as referenced in the text.

Ground and +5v power connections are made through J1 and J2 in parallel. Pins B48, B49, B50 supply the +5v, and pins A48, A49, A50 are used for ground. The PCBA draws approximately 3.25 amps from the +5v supply.

A removable tracking oscillator assembly is mounted at the rear left of the PCBA and mates with a 14-pin IC connector, J4. The oscillator tracks variations in tape speed and compensates the read logic timing accordingly.

A monitor socket, J5 (sheet 3 of 6 zone G5), is provided for maintenance purposes. The various error conditions are wired to this socket and can be individually displayed by use of an oscilloscope.

Three different versions of the Read Recovery PCBA (Assembly 101381) are required to cover the various formatter applications.

(1) Assembly 101380-01 — Standard version. This version consists of a PCBA with a full complement of ICs and is used for single PE formatters, and for dual PE/NRZI formatters which have separate transport interface ports.

(2) Assembly 101380-02 — Transport Terminators Omitted. This version is used on dual PE/NRZI formatters having a common transport interface port.

(3) Assembly 101380-03 — Internal Control Terminators Omitted. Special applications only.

The read logic consists of 9 channels of data logic, and a group of control logic which supervises the reading of each data record.

The design is entirely digital and is based on a tracking oscillator which compensates the read logic timing for average and instantaneous variations in tape speed. The oscillator servos on incoming data such that its

frequency is 24-1/2 times the instantaneous data rate (there are nominally 24-1/2 clock pulses (RCLK) in each phase mode data cell). The oscillator frequency is high in relation to the data rate to achieve the required decoding resolution. Descriptions of the oscillator and tracking control logic are contained in Paragraphs 5.3 and 5.4.

5.6.1 READ DATA INPUT

The transport electronics contains threshold and envelope circuits which require that read signals exceed a minimum amplitude, and persist for four consecutive cell times before being recognized as genuine data. The first four bits of preamble are therefore not transmitted to the formatter logic.

The transport read data lines, IRDP, IRD0-7 (sheet 3 of 6, zone B/E7, G8) are terminated and then fed to one input of a set of nine exclusive OR elements. The second input is controlled by IREV (from the Write PCBA), and causes the data to be either inverted or not, depending on whether the tape is moving in the forward or reverse direction. As a result, any given flux transition on tape appears at the output (RDP, RD0-7) as the same change in signal polarity, regardless of tape direction. This is illustrated in Figure 5-15.

In particular, the data transition for a zero bit appears as a change from low to high, and the data transition for a one-bit appears as a change from high to low.

Operation of the remainder of the read logic is independent of tape direction. Note that the roles of the preamble and postamble are interchanged when reading reverse.

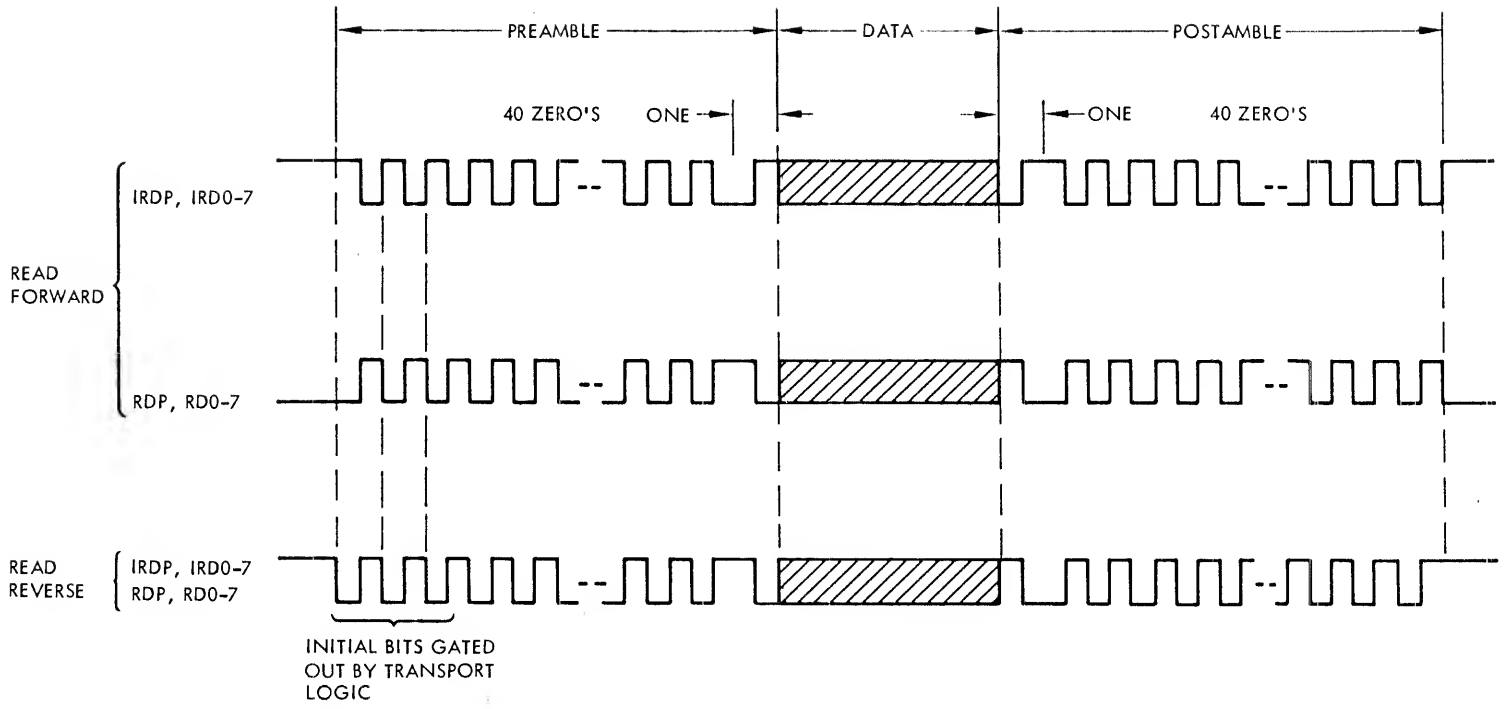


Figure 5-15. Read Input Signals

5.6.2 DATA CHANNEL LOGIC, CIRCUIT DESCRIPTION

RDP, RD0-7 feed 9 sets of data logic which process the information from each track separately. Operation of the data channel logic is discussed with reference to circuit 100 shown on sheet 4 of 6.

The logic is divided into two parts:

(1) Decoding and Deskewing. This includes data decoding, envelope and dropout detection, a 4-bit skew register (S1-4) (sheet 4 of 6, zone E4), and a control register. It accounts for most of the channel logic. The timing of this logic is closely associated with incoming data, and operates independently of the other channels.

(2) Parallel Buffer and Error Correction. This consists of a 2-bit buffer (D1-2) (sheet 4 of 6, zone E3), and gating logic for the insertion of error corrected data. Considering the 9 channels, this provides 2 characters of parallel storage for the assembly and transmission of read data to the controller interface. Data transfers take place simultaneously on all channels.

5.6.2.1 Data Decoding

The decoding method makes use of the self-clocking property of the PE format, i.e., there is a guaranteed data transition at the center of each cell. There may, or may not, be a phase transition depending on the data pattern.

Two steps are required.

(1) A data clock is generated by means of a three-quarter cell timer circuit. When triggered by the data transition the timer remains set until after the phase transition (if

any) has occurred. It is then re-triggered by the following data transition, and this process is repeated each cell-time for the duration of the record. Initial synchronization is performed during the preamble pattern.

(2) The data content (0 or 1) of each cell is decoded by inspecting the polarity of the incoming data shortly after the data transition occurs.

Decoding is accomplished by flip-flops RD1 (A4/15) (sheet 4 of 6, zone E7), RD2 (A4/11) (sheet 4 of 6, zone E6), DSTR (A6/15) (sheet 4 of 6, zone E6), DGATE (A6/11) (sheet 4 of 6, zone C7), a 4-bit ripple counter (A1) (sheet 4 of 6, zone D6), and the associated gates. Decoding waveforms are shown in Figure 5-16. The logic is enabled by a true signal on RGATE when reading is required.

Incoming data on RDP, RD0-7 is synchronized with RCLK (24-1/2 pulses each data cell) at RD1, and then delayed one clock-time by RD2. Appropriate outputs from these flip-flops are gated together to form pulses which mark the positive and negative-going transitions on the input data.

Assume that the first transition is the data transition for a zero bit, as shown in Figure 5-16. The corresponding pulse is gated through A5/6, A7/6 (sheet 4 of 6, zone F6), and causes a pulse to be generated on DSTR (data strobe) during the following clock time. This initiates a delay circuit consisting of DGATE and the 4-bit ripple counter. The DSTR pulse resets the counter, and causes DGATE to set.

The counter proceeds to count 16 RCLK pulses equivalent to a three-quarter cell delay. A count of 16 (rather than 18) is required since a delay of 2 clock-times has already been introduced by DSTR and DGATE.

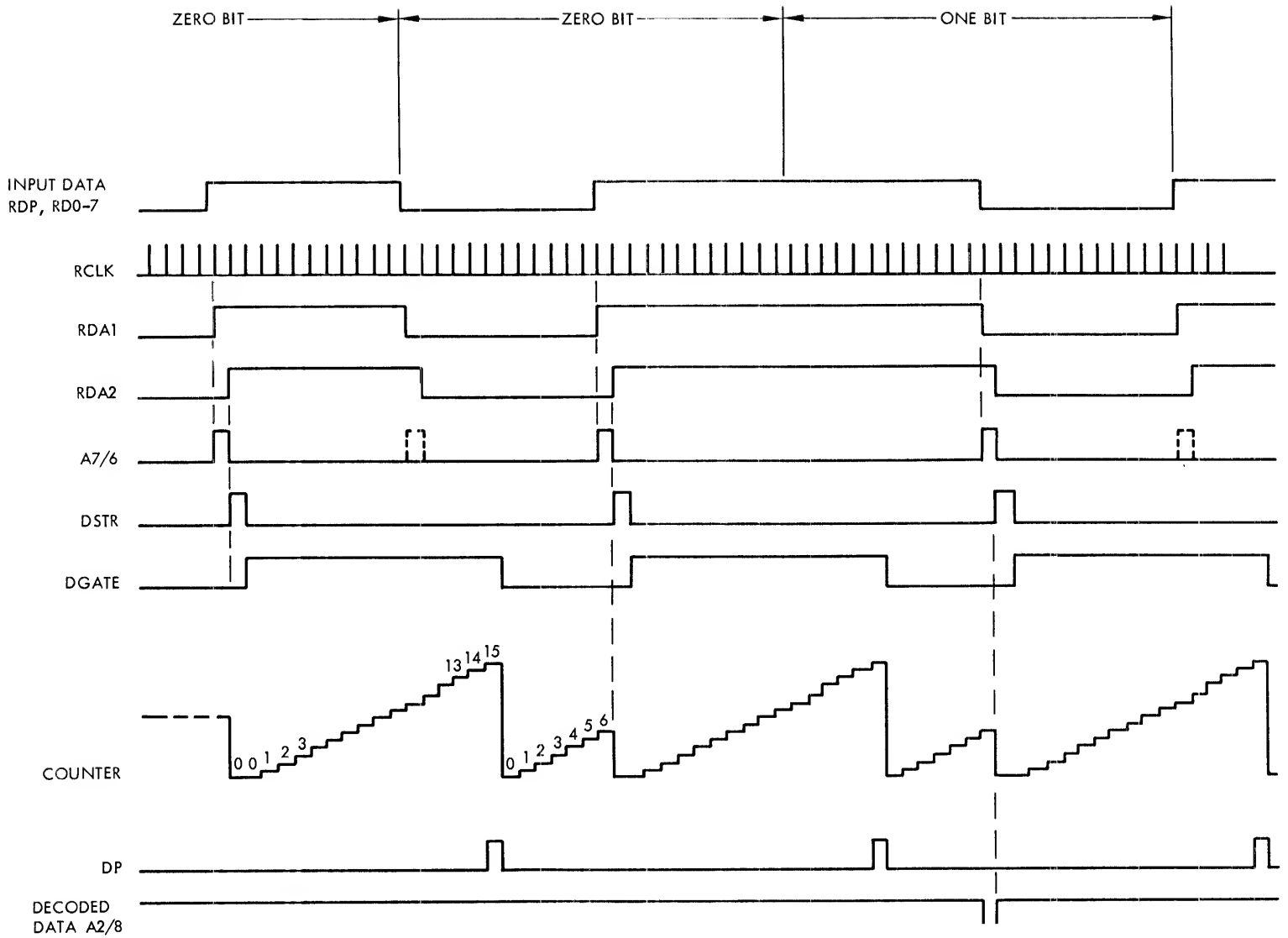


Figure 5-16. Data Decoding Waveforms

During the delay period NRGATE goes low and inhibits A5/6 and A5/8 (sheet 4 of 6, zone E6). This prevents another DSTR pulse being generated as a result of the phase transition.

On the sixteenth clock, a count of 15 (the capacity of the counter) is detected by the ripple counter (A1) and DP goes true. DGATE is now reset, A5/6 and A5/8 are re-enabled, and the delay cycle is complete.

The counter overcarries and continues counting until the data transition for the following cell arrives. Approximately 6 clock pulses are counted (depending on bit crowding and other effects) before the DSTR pulse occurs. A dropout is detected if a count of 15 is reached.

The above sequence is repeated each cell time for the duration of the record. A data clock is formed on DSTR, consisting of one pulse each cell time just after the data transition.

Initial synchronization is performed by the control signal NLO (sheet 4 of 6, zone E8). During the first part of the preamble this waveform disables A5/8, thus preventing the recognition of phase transitions for the preamble zero bits. The logic is therefore forced to synchronize on the data transition.

Data is detected by gating DSTR and NRD2 at A2/8 (sheet 4 of 6, zone E5). This gate goes low at DSTR time when a one-bit is detected. The output is inhibited by NDROP if a dropout has occurred.

5.6.2.2 Envelope and Dropout Detection

Two flip-flops, ENV and DROP (sheet 4 of 6, zone B6, B7) are associated with the decoding logic. The appropriate waveforms are shown in Figure 5-17.

ENV monitors the presence or absence of incoming data throughout each record. It is set by DSTR when data is detected, and reset by A8/4 (sheet 4 of 6, zone C7) when a dropout is detected, i.e., when a count of 15 is reached with DGATE reset. A loss of signal is sensed approximately one-half cell time after a missing data transition was due. In the complete absence of data a reset pulse is generated on A8/4 each time the counter re-cycles.

DROP is enabled by REN1 (sheet 4 of 6, zone A8) from the time of lock-on until mid-way through the postamble. If a dropout is detected during this time the flip-flop is set and the following data from this channel is discarded. Error correction is performed provided that no other channel has experienced a dropout.

5.6.2.3 False Preamble/Postamble Check

Decoded data from A2/8 (sheet 4 of 6, zone F5) is routed through A9/4 (sheet 4 of 6, zone E5) to an open collector inverter A14/2 (sheet 4 of 6, zone D3). The output of this element is collector ORed over the 9 channels to form NONEDET. This goes low when a one bit is decoded on any one of the data channels.

Shortly after lock-on, the error logic inspects this waveform to verify that all channels are successfully decoding the preamble zero bits. A similar check is performed during the first part of the postamble period.

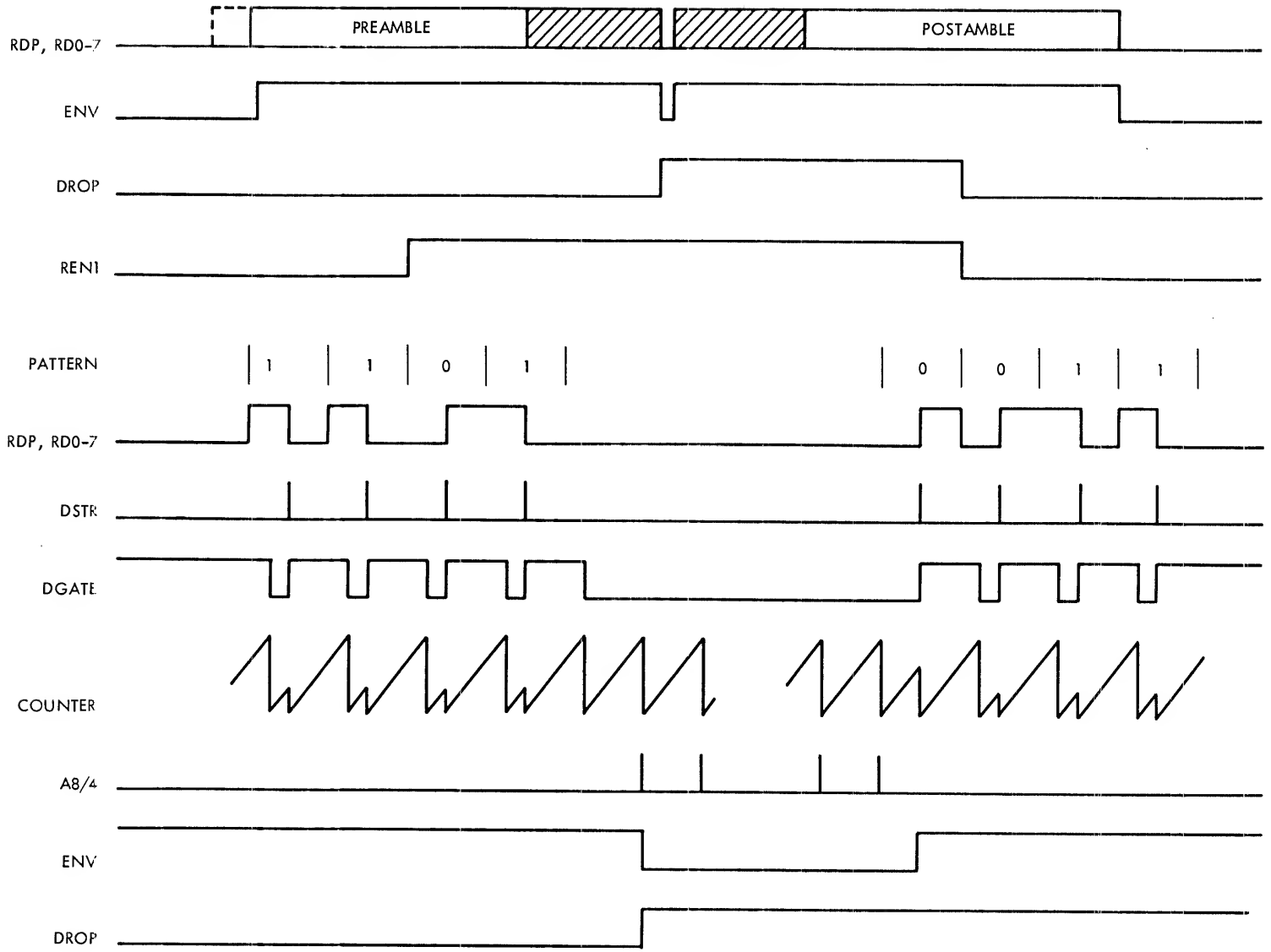


Figure 5-17. Envelope and Drop Waveforms

5.6.2.4 Synchronization Detection

At the end of the preamble test, REN2 (sheet 4 of 6, zone C8) goes true and the synchronous flip-flop (SYNC) is enabled. The first one-bit to be decoded after this time is interpreted as the one-bit at the end of preamble, and causes SYNC to set. (See Figure 5-17).

The bits following the one-bit detected at the end of the preamble are interpreted as data bits until the postamble is detected. A data clock, DSTR SYNC is formed by gating DSTR and SYNC.

5.6.2.5 Data Buffering

The skew register and parallel buffer consist of a 5-bit shift register A13 (sheet 4 of 6, zone E3), and the flip-flop A10/11 (sheet 4 of 6, zone E2). The skew register (S1-4) provides temporary storage for incoming data on each channel until all bits of a character have been assembled. A maximum of 2.9 characters of skew can be tolerated between the 9 channels. When all bits have arrived the character is shifted, in parallel form, to the data buffer (D1-2).

Decoded data is gated with NECLK (sheet 4 of 6, zone F5) then applied to the common input of the skew buffer preset gates. The timing of NECLK is approximately 50 nanoseconds earlier than NRCLK, and makes it possible to enter and shift data in the skew register in the same clock time.

The second input to these gates is controlled by the corresponding stage of a 4-bit shift-left/shift-right register, A12 (sheet 4 of 6, zone G3), which is initially loaded with a one-bit in the right-most (C1) stage. This bit is shifted left or right as required as data is entered or copied from the skew register, so that it "points" to the stage where the next data bit is to be entered.

Shifting is controlled by the following three waveforms.

(1) Mode Control, SHL (A9/12) (sheet 4 of 6, zone D4). This waveform controls the mode select input to the control register. When true, the shift-left mode is selected; when false, the shift-right mode is selected. SHL is set true for one clock time by DSTR SYNC each time a data bit is entered into the skew register. It is also held true by low signals on REN2 and NDROP when it is necessary to clear the control register.

(2) Shift-Left Clock, SLCLK (A11/10) (sheet 4 of 6, zone G5). This waveform consists of a pulse each clock time when SHL is true, except when NCOPY-A is low (when a shift-right operation is required). Each shift pulse causes the contents of the control register to shift left one place. As the shift takes place, the condition (0 or 1) of the control waveform PRESET (sheet 4 of 6, zone H3) is copied into the C1 stage.

(3) Shift-Right Clock, SRCLK (A11/4) (sheet 4 of 6, zone G5). When all bits of a character have been assembled in the skew register, the read control logic generates a low-true pulse on NCOPY-A. This generates a shift-right clock pulse at A11/4 which causes the control register, skew register, and data buffer to shift right one place. This shift takes place simultaneously on all channels. Zero bits are entered into C4 and 54 via A12/1 and A13/9, respectively.

5.6.2.6 Character Detection

The presence of a fully assembled character is detected as follows. The C1 stage of the control register is connected to an open collector inverter whose output is collector ORed for the 9 channels to form the waveform CHDET (character detect) (sheet 4 of 6, zone F2). This waveform goes high only when the control bit in each channel has moved away from the C1 position, i.e., after a data bit has been entered into S1 on all channels. The read control logic detects this condition and generates a pulse on NCOPY-A which causes a shift-right to occur as previously described. The assembled character is copied into D1, and the contents of D1 are transferred to D2. The following character is then assembled in S1.

5.6.2.7 Buffer Overflow

A buffer overflow error is detected by A16/10 (sheet 4 of 6, zone D4) if a data bit is decoded when the control bit is in the C4 position. This occurs if there are three or more characters of skew between this and the latest occurring channel. The DSTR SYNC pulse for this bit causes the control bit to shift out of the control register, resulting in the loss of subsequent data. The output of A14/6 (sheet 4 of 6, zone D4) is collector ORed with a similar signal from the other channels to form a common error signal, NBODET.

5.6.2.8 Postamble Detection

The postamble is detected by decoding the first two postamble characters (a character of all-ones followed by a character of all-zeros). This is performed by A11/13, A11/1, and A14/12 (sheet 4 of 6, zone E2).

A11/13 tests for the required pattern (10) at the output of D1 and S1. If a dropout has occurred, the preamble test for this channel is forced true by the connection of DROP to A11. The result is collector ORed for all channels at A14/12 to form POSTDET.

The read control logic tests POSTDET as each shift-right transfer takes place (when all bits have been assembled in S1). If true, postamble is detected.

5.6.2.9 Buffer Operation

The following buffer sequence takes place when reading each record. Refer to Figure 5-18 for the appropriate waveforms.

The skew register and data buffer are initially dc reset by a low signal on SYNC and REN2. At the same time the control register is cleared by a continuous shift-left operation. Zero bits from the PRESET input cause the register to be cleared.

Midway through the preamble, PRESET goes true for one clock time just before REN2 is set. This causes the control bit to be loaded into the C1 stage of the control register. The input gate of S1 is now enabled.

At the end of the preamble, SYNC goes true and the skew buffer is enabled. One cell time later the first data bit is decoded and is entered into S1. At the same time DSTR SYNC causes the control bit to shift left one place to C2. If this bit is still present when the second bit arrives, the second bit is copied into S2 and the control bit moves to C3, etc.

When all bits of the first character have arrived, a NCOPY-A pulse is issued. The assembled character is shifted from S1 to D1, and the skew and control registers are shifted right one place to make room for new data.

This process is repeated for each data character until postamble is detected. This occurs just before the postamble all-ones character is

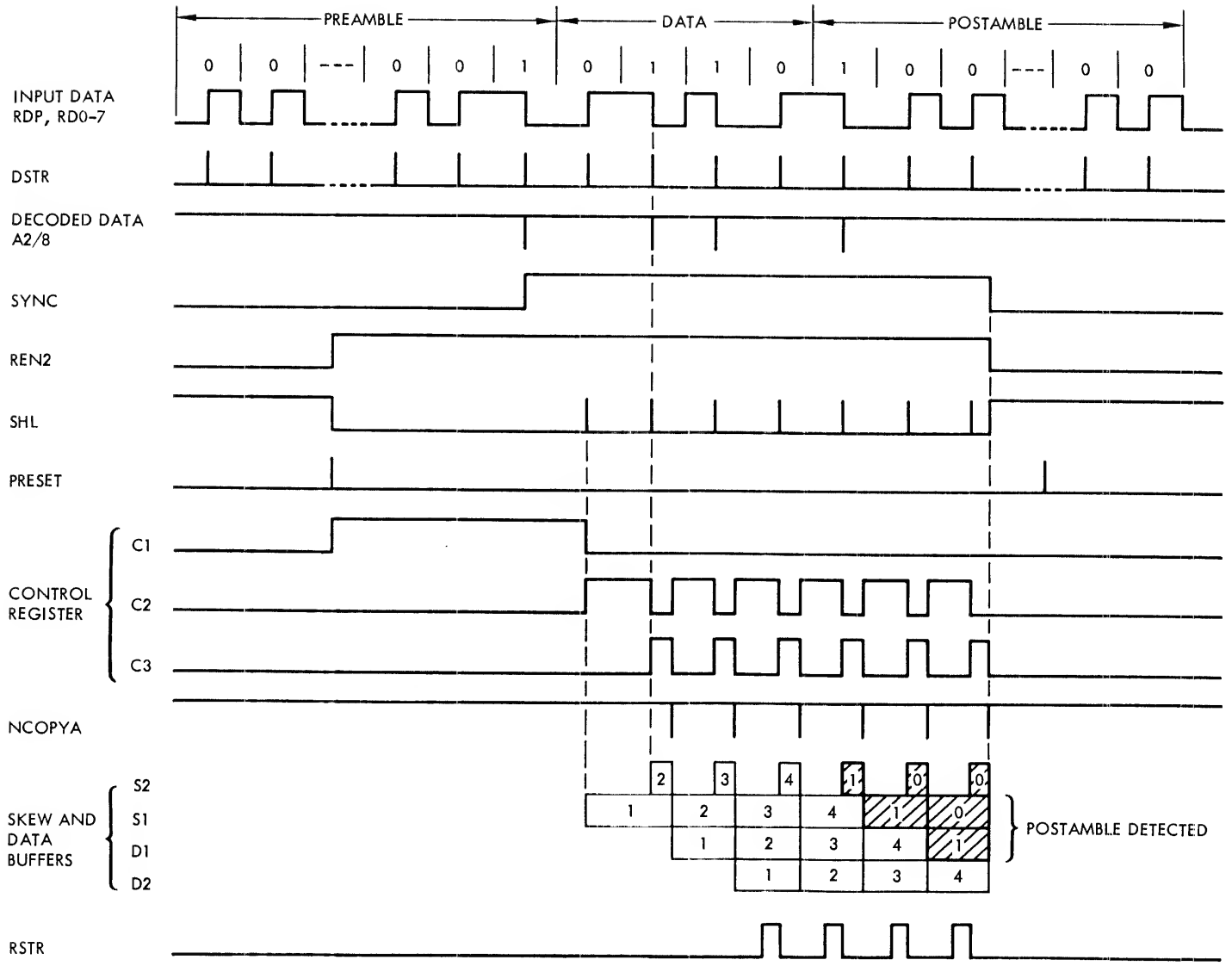


Figure 5-18. Data Buffering

entered into the output (D2) register. REN2 now goes low causing the entire buffer logic to be reset to the initial state.

The decoding logic continues processing postamble information until the end of record is reached.

5.6.2.10 Data Output

Data is taken from both the Q and $\overline{Q}$ outputs of the D2 register.

The Q outputs, DAP, DA0-7, are fed to a parity generator circuit, E17 (sheet 3 of 6, zone C5). If no dropouts have occurred this circuit checks that the parity of each output character is odd. If a single track dropout has occurred the circuit re-generates corrected data for the affected channel, using the data from the other 8 channels.

The $\overline{Q}$ outputs are ORed with corrected data at A15/3 (sheet 4 of 6, zone E2) to form DATA P, DATA 0-7; and then transmitted to the Controller interface read lines, IRP, IR0-7, by driver elements.

A strobe waveform, RSTR, is generated by the read control logic. This consists of a pulse for each data character, and is used to strobe IRP, IR0-7 into the controller logic.

5.6.2.11 Error Correction

Error correction takes place when there has been a single track dropout, and no other error conditions. The following actions take place when the DROP flip-flop is set.

(1) Decoding gate A2/8 (sheet 4 of 6, zone F5) is disabled. This prevents preamble/postamble check errors from being caused by this channel.

(2) SYNC is cleared. This causes S1-S4 and D1 to be cleared. D2 is not affected.

(3) The control register is cleared by a continuous shift left. This channel no longer takes part in character detection (CHDET).

(4) The postamble test is forced true. This channel no longer takes part in postamble detection (POSTDET).

(5) Error correction gate, A15/6 (sheet 4 of 6, zone E2) is enabled.

Error correction does not begin until the next character is transferred to the output buffer. In the meantime, the transmission of the current character (still in D2) to the controller is completed.

When the next character is transferred to D2, a zero bit is copied for the channel in error. At the same time the presence of the dropout is detected by the read control logic. An error correction bit, PARC, is now formed by the parity logic on the basis of the information in the other channels. This is routed through A15/6 and A15/3 on the channel in error to perform the required correction. Correction is performed on each of the following characters until postamble is detected.

The interface line, ICER, indicates to the controller when error correction is taking place.

5.6.3 SINGLE/MULTIPLE TRACK DROPOUT DETECTION

Associated with the data channel logic is a circuit which detects the presence of single or multiple track dropouts.

This takes the output of the nine DROP flip-flops (sheet 3 of 6, zone D3) and forms the following signals.

(1) DROPDET1. This goes high if any one or more of the channels have dropped.

(2) NDROPDET2. This goes low if any two or more of the channels have dropped.

The logic consists of a number of identical circuits, one for each channel. It is broken into two parts, one for Channels P, 0-3, and the other for Channels 4-7. The two halves are then combined by F16/1, F14/4, and F15/8 (sheet 3 of 6, zone D3).

Operation of the Channel 1 stage is as follows. The input from the stage above is an OR of DROP signals from the previous channels in the chain (P and 0). This is ORed with DROP/1 inverted, and then passed on to the following stage. The two signals are also gated at C16/1 (sheet 3 of 6, zone F3) and the result is collector ORed onto the NDROPDET2 line by C14/4 (sheet 3 of 6, zone F3). NDROPDET2 therefore goes low if Channel P has dropped, and either one of Channel P or 0 has dropped.

By repeating this process stage-by-stage the required signals are formed.

5.6.4 CONTROL LOGIC

5.6.4.1 Tracking Control Logic

The tracking control logic generates the control waveforms which servo the tracking oscillator frequency to 24-1/2 times the instantaneous data rate. The decoding waveform DGATE (sheet 5 of 6, zone F8) from Channel 2 is normally used as the tracking input. This waveform goes true for 16 clock times each data cell, and should therefore be false for an average of 8-1/2 clock times before the next data transition occurs. The control logic counts the number of RCLK pulses during this time and generates the appropriate error signal. If Channel 2 drops out, control is automatically switched to Channel 0. Figure 5-19 illustrates the tracking control waveforms.

AND/OR gate E21/8 (sheet 5 of 6, zone E7) selects either DGATE/2 or DGATE/0 as the tracking input depending on whether or not there is input data on Channel 2. The output, TRACKSIG, is then delayed one clock time by B18/15 (sheet 5 of 6, zone E7). When this flip-flop is set, a 3-bit ripple counter (A17/15, A17/11, B17/15) (sheet 5 of 6, zone F6, F7) is enabled, and counts off the number of RCLK pulses which occur during this time. If a count of eight or more is reached the counter overcarries and sets the next flip-flop in line. If the count is less than eight, the flip-flop remains reset. Gates A15/8 and A16/4 (sheet 5 of 6, zone E5, E6) generate a clock pulse which copies the contents of the overflow-flip-flop to B18/11 (sheet 5 of 6, zone F5) during the last clock time before B18/15 goes false.

B18/11 is therefore set or reset each data cell depending on whether the oscillator frequency is too high or too low. The two outputs are inverted to form the oscillator control waveforms NER1 and NER2. When NER1 is low the frequency is decreased; when NER2 is low the frequency is increased.

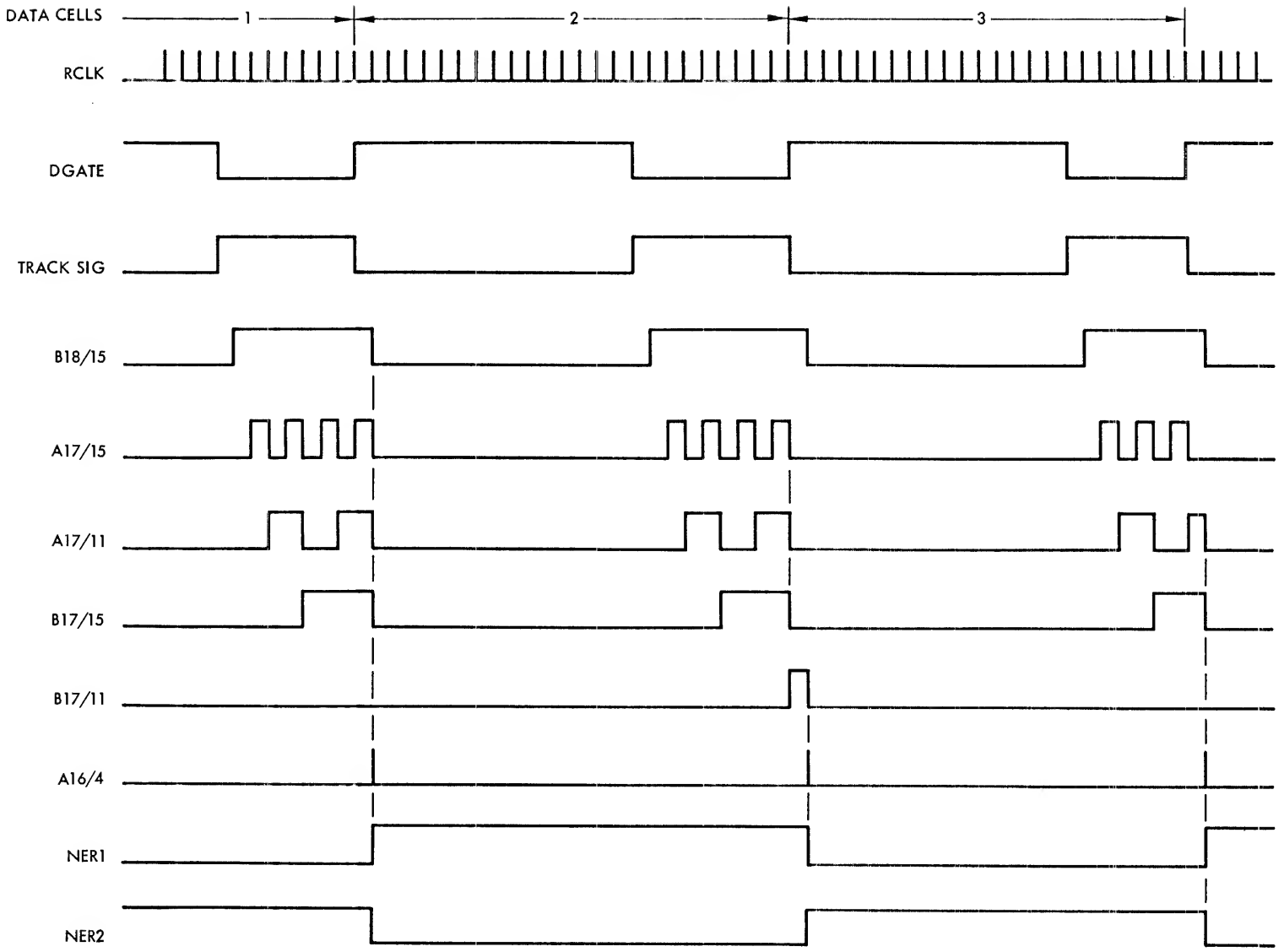


Figure 5-19. Tracking Control Waveforms

In the absence of input data, DATA2 (sheet 5 of 6, zone F5) clamps B18/11 off at the dc set and reset inputs. This causes NER1 and NER2 to go low at the same time, and the tracking oscillator reverts to its center frequency.

5.6.4.2 Clock Distribution

The output from the tracking oscillator is fed to a delay chain of six inverter elements, and then inverted at H17/8 (sheet 5 of 6, zone H5) to form NRCLK. Six power gates, RCLK1-6, distribute the waveform to various parts of the read logic. The relevant area is indicated beneath each waveform name.

The first inverter in the chain, NECLK, is timed approximately 50 ms earlier than NRCLK. This is used to gate decoded data to the skew buffer in the data channel logic. (See Figure 5-20.)

5.6.4.3 Read Enable

IRGATE (sheet 5 of 6, zone E8) is set true by the PE Write PCBA when the reading of a data record is required. This signal is fed to three power gates, RGATE1-3, which drive the 9 channels of data logic. When reading is required, RGATE1-3 go high, and allow the decoding logic in each channel to recognize input data from tape.

For control purposes, the presence of data on either Channel 2 or Channel 0 is used to indicate that data (data record or file mark) are being read from tape. The same two channels are used for tracking control. Envelope waveforms NENV/2 and NENV/0 are ORed at F17/8 (sheet 5 of 6, zone D7) for this purpose. The waveforms NDATA, DATA1, and DATA2 are then formed.

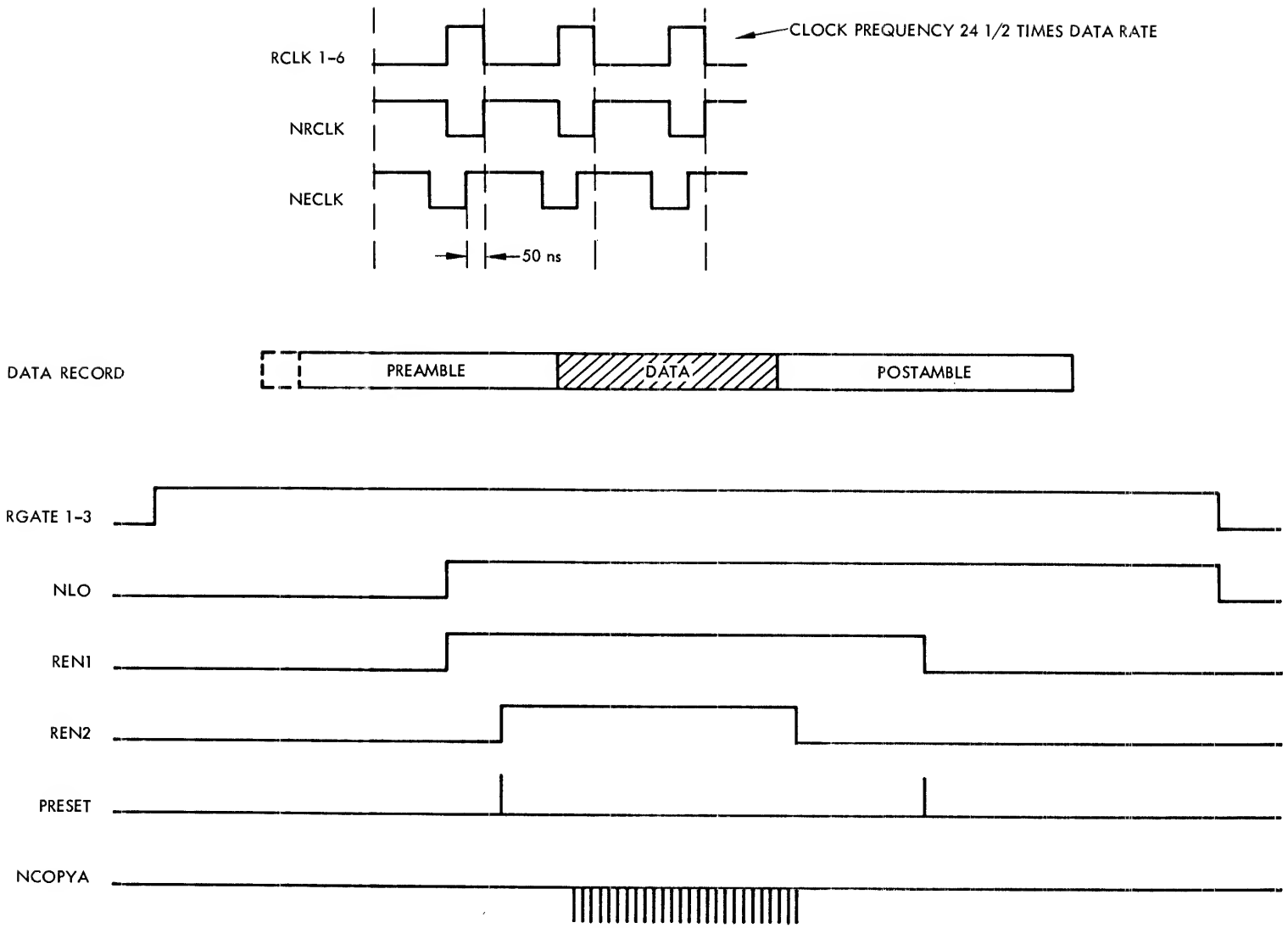


Figure 5-20. Control Signals to Data Channels

When a data pattern begins, DATA2 goes high, and the oscillator begins tracking from its center frequency to the instantaneous data rate. At the same time, NDATA and DATA1 enable the read control logic and allows the initial timing sequence to begin.

5.6.4.4 Sequence Control

Basic timing is provided by a sequence register consisting of 7 flip-flops, RCN1-7 (sheet 6 of 6, zone G3-7), and a counter register RCTR0-11 (sheet 5 of 6, zone D2-5). RCN1-7 set up in turn and mark off the various stages in reading a record. Appropriate control and timing waveforms are derived from the RCN flip-flop counter logic.

The counter logic times out the various delays required during the preamble, postamble, and gap periods, and is also used for data transfer.

The count logic consists of a 12-bit ripple counter (RCTR0-11), a set of decoding gates (F21/8, F20/8, and F20/6) (sheet 5 of 6, zone F2), the flip-flop RP, and the counter reset gates. The counter input (G20/14) (sheet 5 of 6, zone D5) is tied to RCLK so that the counter is always counting except when it is reset by the NOR gate E22/6.

The length of the delay is determined by one of the three decode gates which are ORed into F21/6 (sheet 5 of 6, zone F2). F21/8 is a 22-character delay time and is always enabled. F20/8 is enabled when RCN2 is true and RCN4 is false and has a delay of four character times. F20/6 has a delay of 0.7 character times and is enabled by CCN2 during a read data transfer. When the counter reaches the count of one of the enabled decode gates, RP is set true for one clock time. RP is one of the reset terms of the counter so that the counter is reset to all-zeros at every RP.

The read control sequence (see Figure 5-21) is initiated when the data signal goes true. This removes the reset level from the counter by disabling E21/6 (sheet 5 of 6, zone C3). The counter issues an RP after 22 character times which sets RCN1 and RCN2 true. RCN1 causes NLO to go true and RCN2 causes REN1 to go true. The decode gate F20/8 is now enabled and an RP will be issued after four character times which will set RCN3 true.

During the next four character times, before RCN4 is set true, a test for one bits in the preamble will be made by the AND/NOR gate H22/8 and the NAND gate D22/1 (sheet 6 of 6, zone F7).

When RCN4 goes true, REN2 will be enabled and the decode gate F20/8 will be disabled. The logic is now looking for the all-ones character at the end of the preamble. If it does not occur within 22 character times from the time RCN4 was set true (52 character times from start of read) the NAND gate E20/6 (sheet 6 of 6, zone E7) (NERR3) goes true to indicate a format error.

When the postamble is detected RCN5 will be set true which disables REN2 and enables AND/NOR H22/8 for a ones test of the postamble. After 22 character times RCN6 is set true by RP and REN2 is disabled. At the end of another 22 character times when RCN7 is set true a test is performed by the NAND gate E20/8 (NERR4) to check for the end of data and the start of the gap. RCN7 will be set true for 22 character times during which no data can occur, and RCN7 also resets RCN2-7. At the end of 22 character times the read end pulse (REND) is set true for one clock time; RCN1 is also reset at this time. REND signals the end of the read sequence.

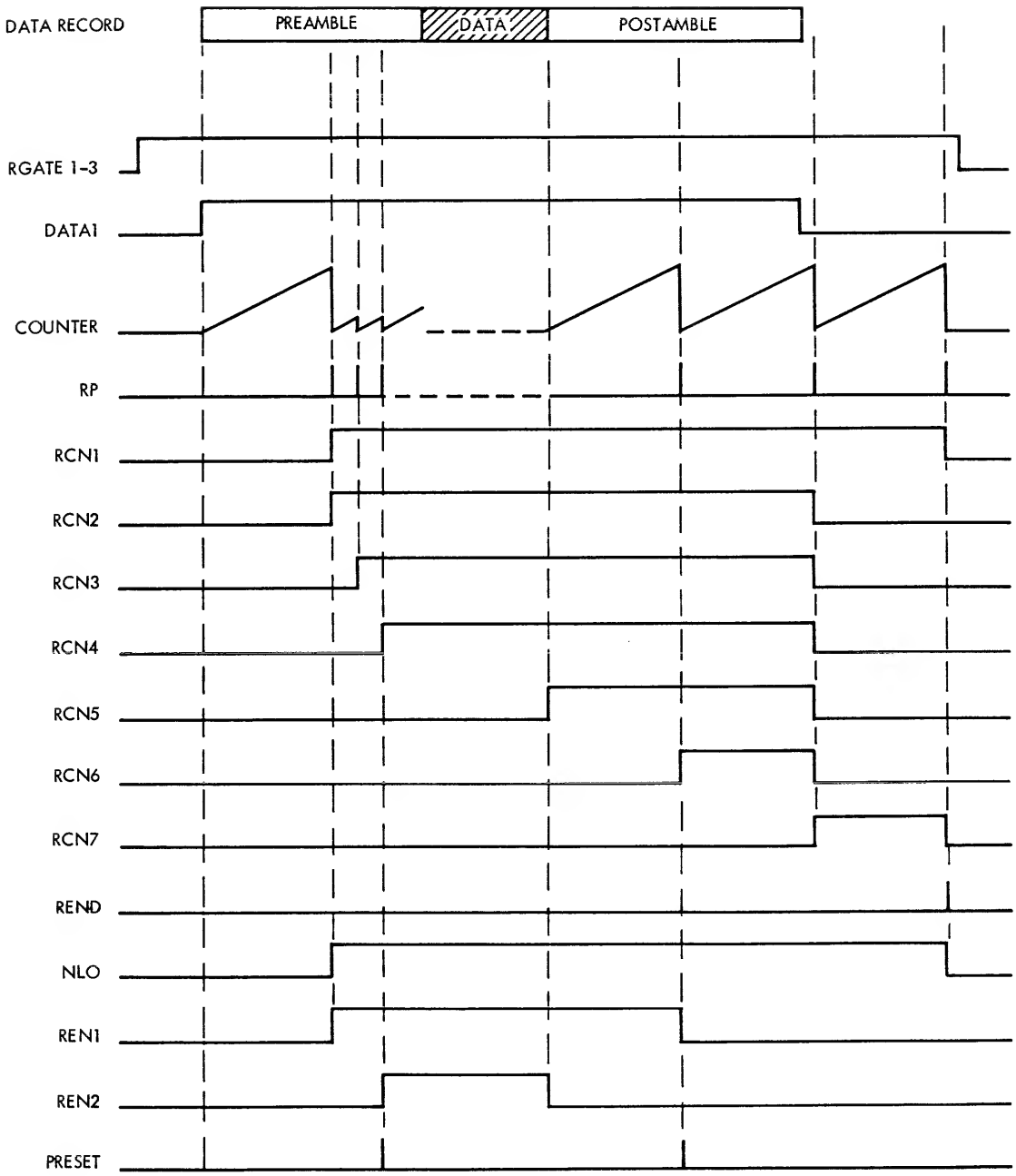


Figure 5-21. Sequence Control

5.6.4.5 Data Control

The data control consists of three flip-flops (COPY, CCN1, and CCN2) (sheet 5 of 6, zone B5, 6, 7) which are enabled when RCN4 goes true. When the first character has been deskewed (see Figure 5-22) Character Detect (CHDET) goes true which sets the COPY flip-flop true for one clock time and shifts the first character into the data buffer. CCN1 is set true on the next clock pulse. The next CHDET will set COPY true for one clock which will shift the first character of the record to the output flip-flop of the data register and set CCN2 true. CCN2 enables the decode gate F20/6 and the NOR gate H19/1 (sheet 5 of 6, zone B2) so that a read strobe (RSTR) will be issued in the center of the data cell. RP will go true 17 clock pulses from the time CCN2 was set true and reset CCN2. When CCN2 is true the NOR gate H19/3 is disabled so that the transfer of the next character will not start until the first character has been transmitted out of the interface.

This sequence of data transfer continues until the all-ones bit of the postamble is shifted into the first stage of the data buffer. The postamble detect signal (POSTDET) will go true and after the last character of the record has been strobed the first character of the postamble will cause COPYCLK to set RCN5 true. RCN5 true will reset all the data control flip-flops.

5.6.5 FILE MARK

A file mark is identified by 40 zeros in Channels P, 0, and 5, with Channels 1, 3, and 4 dc erased. Channels 2, 6, and 7 can be dc erased or have 40 zeros. NAND gates D17/6 and D17/8 (sheet 6 of 6, zone D7) look for data in Channels P, 0, and 5, or 2, 6, and 7. NAND gate F17/6 looks for the absence of data in Channels 1, 3, and 4. At the end of 22 character times from the start of data (see Figure 5-23), RP will set

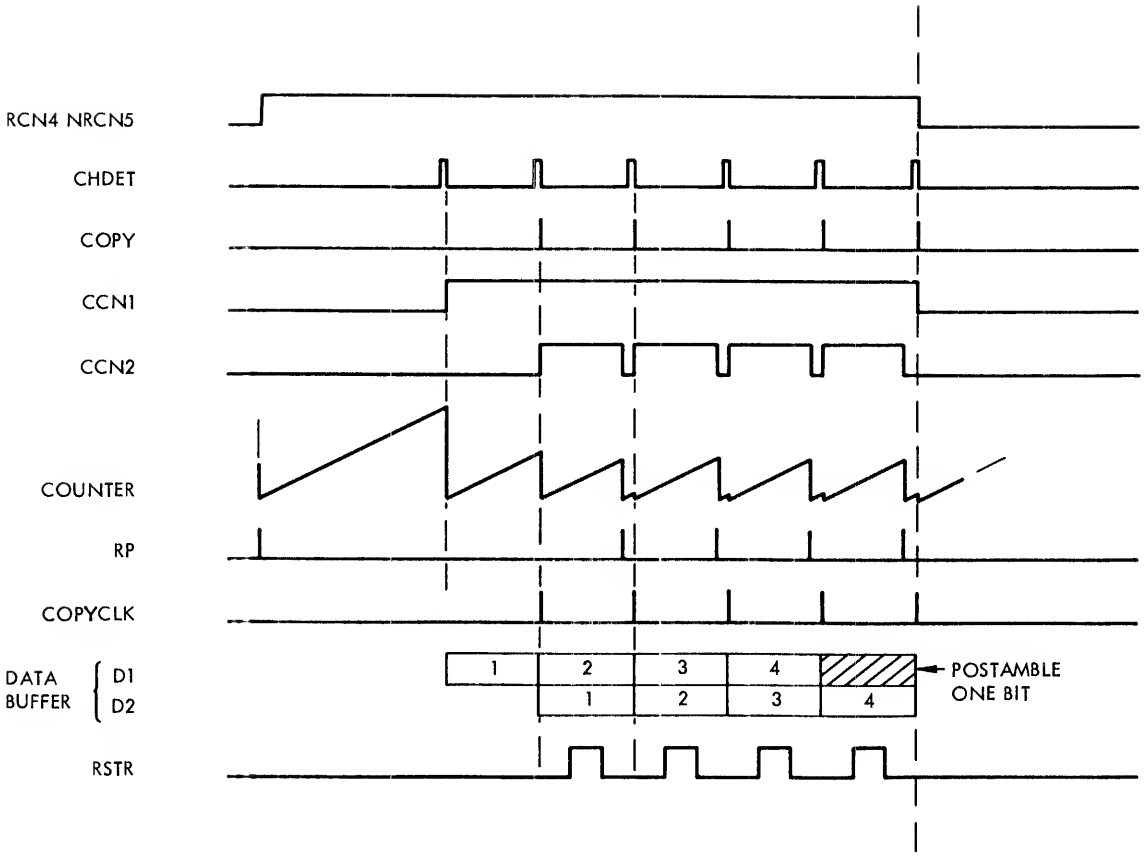


Figure 5-22. Data Control

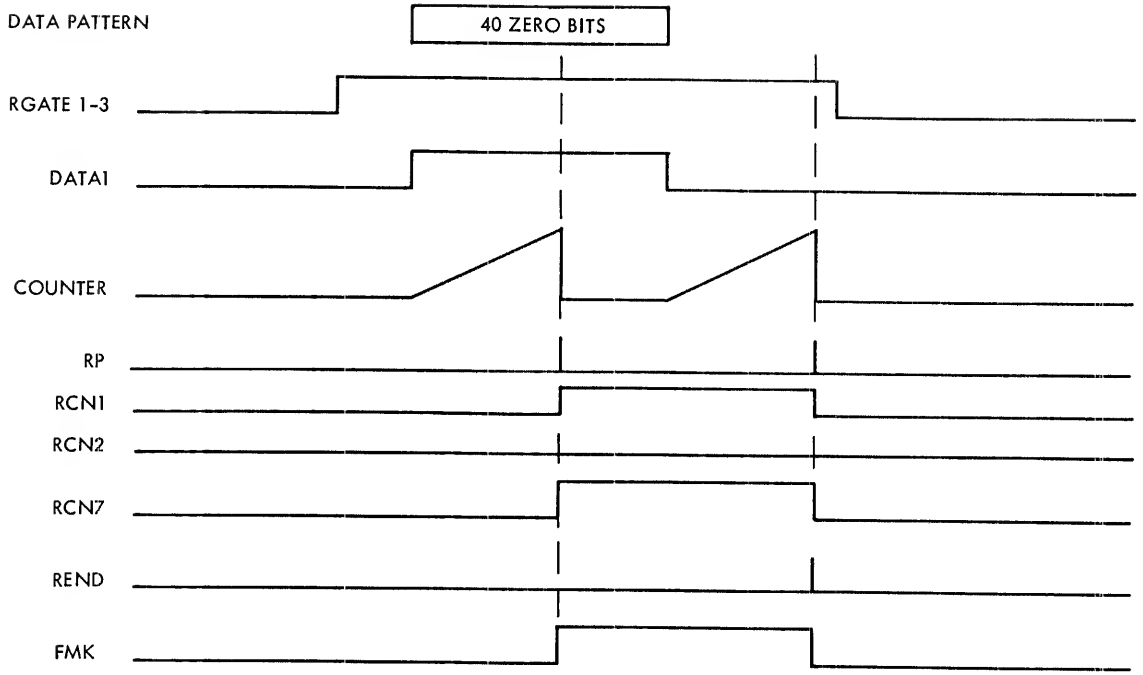


Figure 5-23. File Mark Waveforms

RCN1, RCN2, and FM true. FM going true enables H22/6 (sheet 6 of 6, zone E4) so that RCN7 is set true on the next clock pulse which in turn resets RCN2. The read sequence logic then waits for the end of data at which time the read counter counts for 22 character times and sets REN1 true for one clock time. The REND pulse resets RCN1, RCN7 and the FM flip-flop.

5.6.6 IDENTIFICATION BURST

When the controlled transport is at the beginning of tape (LDP) a test is made for the identification burst. To enable the test IDG (sheet 5 of 6, zone D8) goes true which causes RGATE to go true so that the front half of all the channels are enabled, NLO is held false because the identification burst is a 1 0 1 0 1 pattern and DATA is held false so that the control logic is disabled. Half way through the IDG waveform ITESTID is set true and the NOR gate D16/13 (sheet 6 of 6, zone A7) looks for data on Channel P and no data on Channels 1, 3, and 4. If these conditions are met the interface signal IDENT is set true. After the identification test is completed IDG and ITESTID are reset and IRGATE is set true so that the control logic will read the first record.

5.6.7 ERROR DETECTION

Hard errors (i.e., uncorrectable errors) are of two types; parity errors and format errors. Parity errors are checked with the parity generator IC, E17/6 (sheet 3 of 6, zone C5), which generates odd parity of Channels DA/0 through DA/7 and compares it with the data from the parity Channel (DA/P). If the compare fails, the PE line goes true and the NAND gate D21/8 (sheet 6 of 6, zone B4) will be enabled during the read strobe for the character in error. Therefore, the IHER interface line will be pulsed at the same time the IRSTR pulse strobes the character into the controller if the character had a parity error. The strobed parity error

line is available on pin 3 of the test connector J5 (NER1) for maintenance and test purposes.

Format errors are indicated by the flip-flop F22/11 (FE) (sheet 6 of 6, zone E6) going true which sets the IHER interface line true and forces the logic to look for the end of the record by setting RCN7 true. With RCN7 true a REND pulse will be issued when the DATA signal is false for 22 continuous character times.

The FE flip-flop is set true by one of the four inputs to the NAND gate E22/8 (sheet 6 of 6, zone E6). NDROPDET2 goes low when two or more channels have lost synchronization. This can occur any time after the lock-on signal (NLO) has gone false. The NERR2 input is the combination of a buffer overflow error and the test for ones in the preamble and postamble. The buffer overflow error (NBODET) indicates that one of the channels has more bits of data than it can store. A test is made for ones in the preamble during the four character times DCN3 is true and DCN4 is false and the same is performed during the first 22 character times of the postamble when RCN5 is true and RCN6 is false. If, during these test periods, a one bit appears in any of the channels the NONEDET signal will go low and enable D22/1 (sheet 6 of 6, zone F7).

NERR3 going low indicates that the first data character of the record was not transmitted within 22 character times from the time RCN4 was set true. This error occurs when one or more of the channels fails to detect the one bit at the end of the preamble.

NERR4 is a test to verify that gap at the end of the postamble is within 44 character times from the start of the postamble. This test checks that a false postamble was not detected in the center of a record.

5.6.8 ERROR CORRECTION

If one of the channels looses synchronization during the record, DROPDET 1 will set the flip-flop (D23/15) (sheet 6 of 6, zone B6) CORRECT true. The CORRECT flip-flop true enables D21/6 (sheet 6 of 6, zone B4) which causes the reconstructed data from the parity generator to feed to all the channels via the PARC line. At the same time the parity error NAND gate D21/8 (sheet 6 of 6, zone B4) is disabled by the correct flip-flop and IHER interface line is set true.

SECTION VI
MAINTENANCE ADJUSTMENTS

6.1 INTRODUCTION

This section provides information necessary to perform maintenance adjustments and parts replacement. Sections IV and V contain the theory of operation and schematics required for reference when electrical adjustments or troubleshooting are necessary.

6.2 FUSE REPLACEMENT

Fuses are located on the Power Supply assembly at the front of the formatter.

Line Fuse: 1 amp, S. B.
DC Fuse: 5 amp, F. B.

6.3 SCHEDULED MAINTENANCE

The formatter is designed to operate with a minimum of maintenance and adjustments and replacement of parts is designed to be as simple as possible. Repair equipment is kept to a minimum and only simple tools (e. g. Phillips-head screwdriver, standard screwdriver) are required in most cases.

6.4 CLEANING THE FORMATTER

The formatter PCBAs may require periodic cleaning to remove accumulated dust. It is recommended that a low-pressure air source be employed for this purpose.

To clean the front panel, use a lint-free cloth moistened in isopropyl alcohol.

6.5 PARTS REPLACEMENT ADJUSTMENTS

When it is necessary to repair or replace a major formatter assembly (e.g., Power Supply, Read PCBA, Write PCBA, Read/Write PCBA) the basic adjustments described in Paragraphs 6.6 through 6.6.6.4 should be performed.

6.6 ELECTRICAL ADJUSTMENTS

The following paragraphs describe the test configurations, test procedures, and related adjustments within the formatter.

The following test equipment (or equivalent) is required.

(1) Oscilloscope, Tektronix 561 (or equivalent), vertical and horizontal sensitivity specified to ±3 percent accuracy.

(2) Digital Volt Meter, Fairchild 7050, ±0.1 percent specified accuracy.

(3) Monsanto Counter Timer Model 100-B.

6.6.1 ADJUSTMENT PHILOSOPHY

Acceptable limits are defined in each adjustment procedure, taking into consideration the assumed accuracy of the test equipment specified in Paragraph 6.6.

When the measured value of any parameter is within the acceptable limits NO ADJUSTMENT should be made. Should the measured value fall outside the specified acceptable limits, adjustments should be made in accordance with the relevant procedure. When adjustments are made, the value set should be the exact value specified (to the best of the operator's ability).

6.6.2 POWER SUPPLY PCBA

Potentiometer R4 is employed to adjust the +5v power supply. Refer to Schematic No. 101335 and Assembly No. 101336.

NOTE

The +5v supply must be checked and adjusted, if necessary, prior to adjusting the Fixed Frequency Oscillator or the Tracking Oscillator.

6.6.2.1 Test Configuration

(1) Loosen the two captive screws located on the front panel and extend the formatter unit.

(2) Depress and release the spring-loaded button located on the right side of the unit. This permits the front panel to swing down.

(3) Remove the four Phillips-head screws securing the perforated cover to the formatter assembly. The cover can now be removed.

(4) Ensure that all relevant PCBAs are installed and properly seated.

6.6.2.2 Test Procedure

NOTE

The ground (GND) and the +5v test points are located at the rear of the PCBA adjacent to J2.

(1) Using a Fairchild 7050 Digital Volt Meter (or equivalent) measure the voltage between the GND (0v) and the +5v test points on the topmost installed PCBA as follows.

- PE Write/Control, Assembly No. 101386
- PE Read, Assembly No. 101381
- NRZI Read/Write, Assembly No. 101623

(2) Acceptable limits.

- +5.1v maximum
- +4.9v minimum

6.6.2.3 Adjustment Procedure

When the acceptable limits are exceeded, adjust potentiometer R4, located on the Power Supply PCBA as follows.

(1) Monitor the voltage between the GND (0v) and the +5v test point on the topmost installed PCBA.

(2) Adjust R4 to +5v.

6.6.2.4 Related Adjustments

The Fixed Oscillator and Tracking Oscillator must be checked and adjusted when adjustments are made to the +5v power supply.

6.6.3 FIXED OSCILLATOR (SINGLE SPEED FORMATTER)

A fixed frequency oscillator is employed on the NRZI Read/Write PCBA and the PE Write/Control PCBA. Refer to the relevant schematic and assembly drawing.

NOTE

The +5v power supply should be checked and adjusted prior to checking the Fixed Oscillator.

6.6.3.1 Test Configuration

Establish test configuration outlined in Paragraph 6.6.2.1.

6.6.3.2 Test Procedure

(1) Calculate the appropriate frequency for the Fixed Oscillator as follows.

(a) NRZI

- Frequency (KHz) = 14.4 × Speed (ips)

(b) PE

- Frequency (KHz) = 9.6 × Speed (ips)

(2) Record the operating frequency of the oscillator as measured between TP4 and TP1 (0v) on the Single Fixed Oscillator using a Monsanto Counter Timer Model 100-B (or equivalent).

(3) Acceptable limits.

- ±0.5 percent of value calculated in Step (1).

6.6.3.3 Adjustment Procedure

When the measured frequency exceeds the acceptable limits proceed as follows.

(1) Connect a Monsanto Counter Timer Model 100-B (or equivalent) between TP4 and TP1 (0v) on the Single Fixed Oscillator.

(2) Adjust potentiometer R5, located on the Fixed Oscillator assembly, until the measured frequency equals the calculated oscillator frequency (refer to Paragraph 6.6.3.2).

6.6.3.4 Related Adjustments

- None

6.6.4 FIXED OSCILLATOR (DUAL SPEED FORMATTER)

Formatters designed to operate with transports of different speeds are equipped with a dual fixed oscillator. Refer to the relevant schematic and assembly drawing.

NOTE

The +5v power supply should be checked and adjusted prior to checking the Fixed Oscillator.

6.6.4.1 Test Configuration

Establish test configuration outlined in Paragraph 6.6.2.1.

6.6.4.2 Test Procedure

(1) Set the ISPEED interface line false. This enables the oscillator circuitry designed to operate at the higher of the two specified frequencies.

(2) Calculate the appropriate frequency for the Fixed Oscillator as follows.

(a) NRZI

- Frequency (KHz) = 14.4 × Speed (ips)

(b) PE

- Frequency (KHz) = 9.6 × Speed (ips)

(3) Record the operating frequency of the oscillator as measured between TP4 and TP1 (0v) on the Single Fixed Oscillator using a Monsanto Counter Timer Model 100-B (or equivalent).

(4) Acceptable limits.

- ±0.5 percent of value calculated in Step (2).

(5) Set the ISPEED interface line true. This enables the oscillator circuitry designed to operate at the lower of the two specified frequencies.

(6) Repeat Steps (2) through (4) above.

6.6.4.3 Adjustment Procedure

When the measured frequency exceeds the acceptable limits proceed as follows.

(1) Set the ISPEED interface line false.

(2) Connect a Monsanto Counter Timer Model 100-B (or equivalent) between TP4 and TP1 (0v) on the Fixed Oscillator assembly.

(3) Adjust potentiometer R5, located on the Fixed Oscillator assembly until the measured frequency equals the higher of the calculated oscillator frequencies (refer to Paragraph 6.6.3.2).

(4) Set the ISPEED interface line true.

(5) Adjust potentiometer R17, located on the Fixed Oscillator assembly until the measured frequency equals the lower of the calculated oscillator frequencies (refer to Paragraph 6.6.3.2).

6.6.4.4 Related Adjustments

- None

6.6.5 TRACKING OSCILLATOR (SINGLE SPEED FORMATTER)

A tracking oscillator is employed on the PE Read Recovery PCBA. Refer to the relevant schematic and assembly drawing.

NOTE

The +5v power supply should be checked and adjusted prior to checking the Fixed Oscillator.

6.6.5.1 Test Configuration

(1) Establish test configuration outlined in Paragraph 6.6.2.1.

(2) Ensure that the formatter is in an inactive state, i.e., controlled transports not performing a read or write function.

6.6.5.2 Test Procedure

(1) Calculate the appropriate center frequency for the tracking oscillator as follows.

(a) PE PCBA Version

- Frequency (KHz) = 39.2 × Speed (ips)

(b) PE Wire Wrap Version

- Frequency (KHz) = 37.6 × Speed (ips)

(2) Record the center frequency of the oscillator measured between TP4 and TP1 on the Tracking Oscillator assembly using a Monsanto Counter Timer Model 100-B (or equivalent).

(3) Acceptable limits.

- ±1 percent of value calculated in Step (1).

6.6.5.3 Adjustment Procedure

When the measured frequency exceeds the acceptable limits proceed as follows.

(1) Connect a Monsanto Counter Timer Model 100-B (or equivalent) between TP4 and TP1 (0v) on the Tracking Oscillator assembly.

(2) Adjust potentiometer R5, located on the Tracking Oscillator assembly until the measured frequency equals the calculated oscillator frequency (Paragraph 6.6.5.2).

6.6.5.4 Related Adjustments

- None

6.6.6 TRACKING OSCILLATOR (DUAL SPEED FORMATTER)

Formatters designed to operate with transports of different speeds are equipped with a dual speed tracking oscillator. Refer to the relevant schematic and assembly drawing.

NOTE

The +5v power supply should be checked and adjusted prior to checking the Tracking Oscillator.

6.6.6.1 Test Configuration

(1) Establish test configuration outlined in Paragraph 6.6.2.1.

(2) Ensure that the formatter is in an inactive state, i.e., controlled transports not performing a read or write function.

6.6.6.2 Test Procedure

(1) Set the ISPEED interface line false. This enables the oscillator circuitry designed to operate at the higher of the two specified frequencies.

(2) Calculate the appropriate center frequency for the Tracking Oscillator as follows.

(a) PE PCBA Version

- Frequency (KHz) = 39.2 × Speed (ips)

(b) PE Wire Wrap Version

- Frequency (KHz) = 37.6 × Speed (ips)

(3) Record the center frequency of the oscillator measured between TP4 and TP1 on the Tracking Oscillator assembly using a Monsanto Counter Timer Model 100-B (or equivalent).

(4) Set the ISPEED interface line true. This enables the oscillator circuitry designed to operate at the lower of the two specified frequencies.

(5) Record the center frequency of the oscillator measured between TP4 and TP1 on the Tracking Oscillator assembly using a Monsanto Counter Timer Model 100-B (or equivalent).

(6) Acceptable limits.

- ±1 percent of value calculated in Step (1).

6.6.6.3 Adjusted Procedure

When the measured frequency exceeds the acceptable limits proceed as follows.

(1) Set the ISPEED interface line false.

(2) Connect a Monsanto Counter Timer Model 100-B (or equivalent) between TP4 and TP1 (0v) on the Tracking Oscillator assembly.

(3) Adjust potentiometer R5 located on the Tracking Oscillator assembly until the measured frequency equals the higher of the calculated oscillator frequency (Paragraph 6.6.6.2).

(4) Set the ISPEED interface line true.

(5) Adjust potentiometer R17 located on the Tracking Oscillator assembly until the measured frequency equals the lower of the calculated oscillator frequency (Paragraph 6.6.6.2).

6.6.6.4 Related Adjustments

- None

SECTION VII
SCHEMATICS AND PARTS LISTS

7.1 INTRODUCTION

This section includes the schematics, assembly drawings, parts lists, and logic level and waveform definitions.

7.2 SPARE PARTS

Table 7-1 provides a description of the spare parts. When ordering spare parts customer should include model and serial number of the formatter.

7.3 PART NUMBER CROSS REFERENCE

Table 7-2, Part Number Cross Reference, provides a cross reference to the manufacturer part numbers and PERTEC part numbers.

Table 7-1

Spare Parts List

Item	Part No.
1. PE Formatter, Read PCBA	101381-01
2. PE Formatter, Write PCBA	101386-01
3. NRZI 7/9 Read/Write PCBA	101623-01
4. Interconnect PCBA	101367-02
5. Fixed Oscillator PCBA (PE 25 ips)	102096-05
6. Fixed Oscillator PCBA (NRZI 25 ips, PE 37.5 ips)	101362-06
7. Fixed Oscillator PCBA (PE 12.5 ips)	101362-03
8. Fixed Oscillator PCBA (PE 22.5 ips)	101362-05
9. Fixed Oscillator PCBA (PE 18.75 ips, NRZI 12.5 ips)	101362-04
10. Fixed Oscillator PCBA (NRZI 25 ips)	102096-06
11. Tracking Oscillator PCBA (PE 37.5 ips)	101395-01
12. Tracking Oscillator PCBA (PE 25 ips)	101395-02
13. Tracking Oscillator PCBA (PE 12.5 ips)	101395-04
14. Tracking Oscillator PCBA (PE 22.5 ips, Dual)	101395-09
15. Tracking Oscillator PCBA (PE 25 ips)	102094-02
16. Power Supply Assembly	101314-01
17. Power Supply PCBA	101336-01
18. Switch, Rocker	506-0808
19. Fuse, 1 amp, S. B.	663-3510
20. Fuse, 5 amp, F. B.	663-3050
21. Extender Board	101595-01

Table 7-2

Part Number Cross Reference

PERTEC Part No.	Manufacturer	Manufacturer Part No.* and Description
Capacitors		
130-2215	QPL	DM-15-100J (220pf, 500v dc, 5%)
130-4715	QPL	DM-15-471J (470pf, 500v dc, 5%)
131-1020	Callins Ind.	424B102K (0.001μf, 100v dc, 10%)
131-1030	Callins Ind.	424B103K (0.01μf, 100v dc, 10%)
131-1040	Callins Ind.	424B104K (0.1μf, 100v dc, 10%)
131-2230	Callins Ind.	424B222K (0.022μf, 100v dc, 10%)
131-3320	Callins Ind.	424B332K (0.0033μf, 100v dc, 10%)
132-2752	Components, Inc.	EG35-275-10 (2.7μf, 35v dc, 20%)
133-7060	Mallory	MTA70E20 (70μfd, 20v dc, -10 +100%)
134-3000	STM	60C15BAS33 (3000μfd, 15v dc)
134-8000	STM	91C25HC822 (8000μfd, 25v dc)
Diodes		
300-4446	Components, Inc.	1N4446
Diodes, Zener		
330-0685	Motorola	1N4736A
Integrated Circuits		
700-4180	Texas Instr.	SN74180N (8-bit odd/even parity generator)
700-7400	Texas Instr.	SN7400N (Quad 2 input, NAND)
700-7402	Texas Instr.	SN7402N (Quad 2 input, NOR)
700-7404	Texas Instr.	SN7404N (Hex Inverter)
700-7416	Texas Instr.	SN7416N (Hex Buffer Inverter)
700-7420	Texas Instr.	SN7420N (Dual 4 Input NAND)

*or equivalent

Table 7-2

Part Number Cross Reference (cont'd)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* and Description
IC's (cont'd)		
700-7430	Texas Instr.	SN7430N (8 Input NAND)
700-7440	Texas Instr.	SN7440N (Dual 4 Input NAND Buffer)
700-7450	Texas Instr.	SN7450N (Expandable Dual 2 Wide 2 Inputs and/or Inverter Gates)
700-7476	Texas Instr.	SN7476N (Dual J-K Flip-Flop)
700-7486	Texas Instr.	SN7486N (Quad 2 Input Exclusive OR Gate)
700-7493	Texas Instr.	SN7493N (4-Bit Binary Counters)
700-7495	Texas Instr.	SN7495N (4-Bit Right Shift, Left Shift Registers)
700-7496	Texas Instr.	SN7496N (5-Bit Shift Register)
700-8360	Texas Instr.	SN15836N (Hex Inverter)
700-8440	Texas Instr.	SN15844N (DTL IC)
Rectifiers		
201-3228	RCA	2N3228 (TO-66)
201-4654	RCA	40654 (TO-5)
Resistors, Carbon Comp	QPL	
100-1015	QPL	RC07GF101J (1/4W, 5%, 100 ohms)
100-1025	QPL	RC07GF102J (1/4W, 5%, 1000 ohms)
100-1035	QPL	RC07GF103J (1/4W, 5%, 10K)
100-1515	QPL	RC07GF151J (1/4W, 5%, 150 ohms)
100-2205	QPL	RC07GF220J (1/4W, 5%, 22 ohms)
100-2215	QPL	RC07GF221J (1/4W, 5%, 220 ohms)
100-2225	QPL	RC07GF222J (1/4W, 5%, 2.2K)
100-2235	QPL	RC07GF223J (1/4W, 5%, 22K)
100-3305	QPL	RC07GF330J (1/4W, 5%, 33 ohms)

Table 7-2

Part Number Cross Reference (cont'd)

PERTEC Part No.	Manufacturer	Manufacturer Part No.* and Description
Resistors, CC (cont'd)		
100-3325	QPL	RC07GF332J (1/4W, 5%, 3.3K)
100-4715	QPL	RC07GF471J (1/4W, 5%, 470 ohms)
100-5625	QPL	RC07GF562J (1/4W, 5%, 5.6K)
100-5635	QPL	RC07GF563J (1/4W, 5%, 56K)
100-6815	QPL	RC07GF681J (1/4W, 5%, 680 ohms)
100-6825	QPL	RC07GF682J (1/4W, 5%, 6800 ohms)
101-1005	QPL	RC20GF100J (1/2W, 5%, 10 ohms)
101-1025	QPL	RC20GF102J (1/2W, 5%, 1.0K)
101-1825	QPL	RC20GF182J (1/2W, 5%, 1.8K)
101-2705	QPL	RC20GF270J (1/2W, 5%, 27 ohms)
102-6815	QPL	RC32GF681J (1W, 5%, 680 ohms)
110-0011	Dale Electr., Inc.	RS-10 (10W, 3%, 0.1 ohm)
Resistors, Variable		
121-1020	Helipot Div., Beckman Instr.	79PR1K (1K, 3/4W, 10%)
Sockets		
503-7541	AMP, Inc.	583529-1 (16-pin, IC, solder terminal)
503-7544	AMP, Inc.	583527-1 (14-pin, IC, solder terminal)
503-7613	AMP, Inc.	1-380852-0 (16-pin, IC, wire wrap)
503-8358	AMP, Inc.	1-380845-0 (14-pin, IC, wire wrap)

Table 7-2

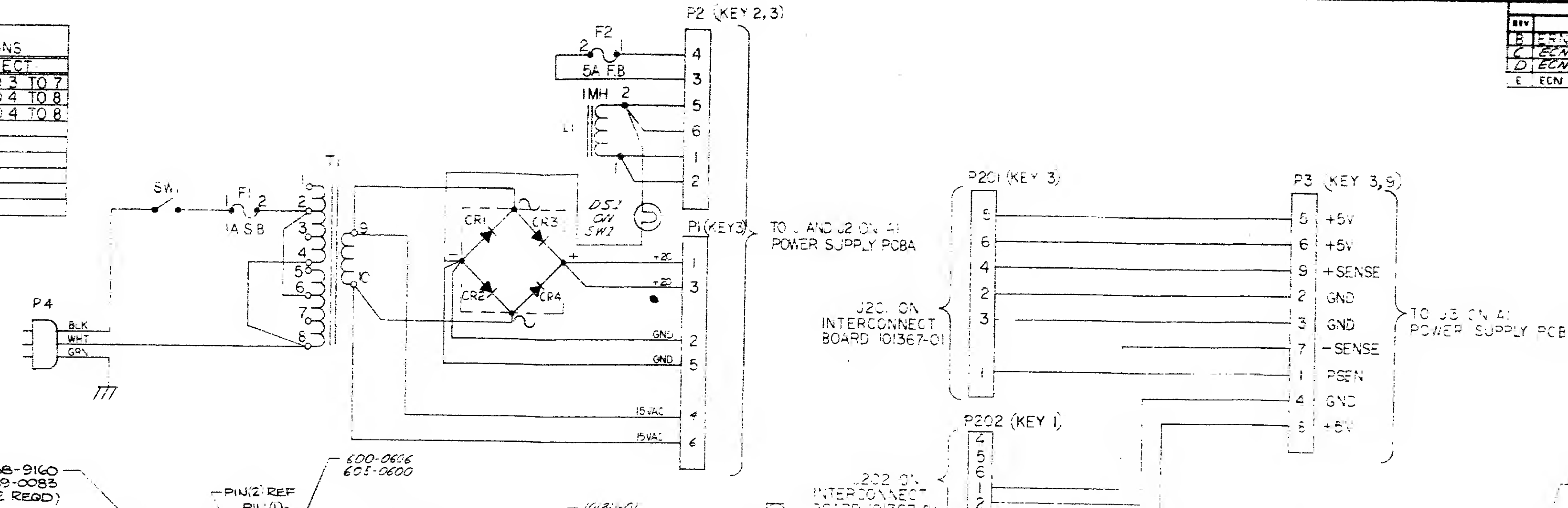
Part Number Cross Reference (cont'd)

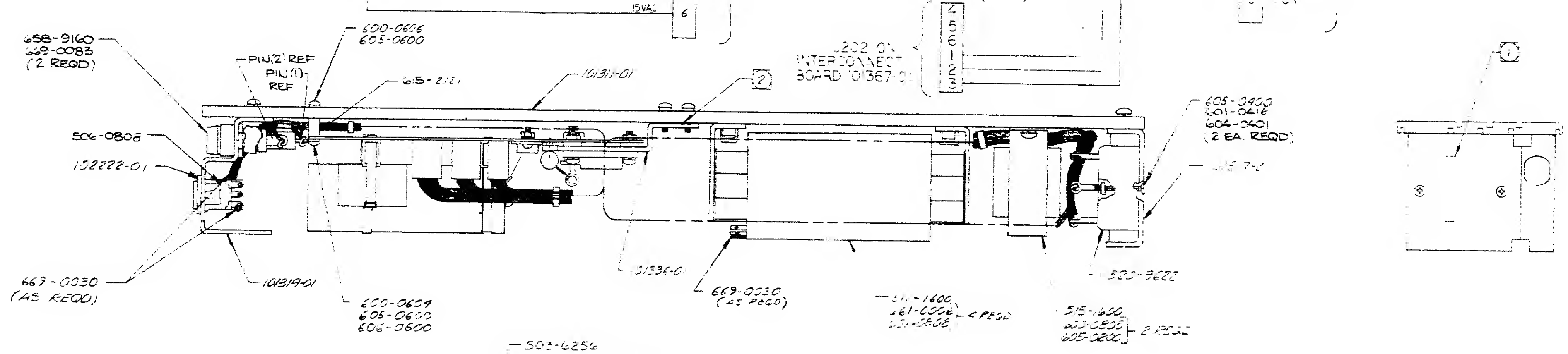
PERTEC Part No.	Manufacturer	Manufacturer Part No.* and Description
Transistors		
200-3053	Motorola	2N3053 (NPN)
200-3055	Motorola	2N3055 (NPN)
200-3771	Motorola	2N3771 (NPN)
200-4037	RCA	2N4037 (NPN)
200-4123	Motorola	2N4123 (NPN, Switching)
200-4125	Motorola	2N4125 (PNP, Switching)

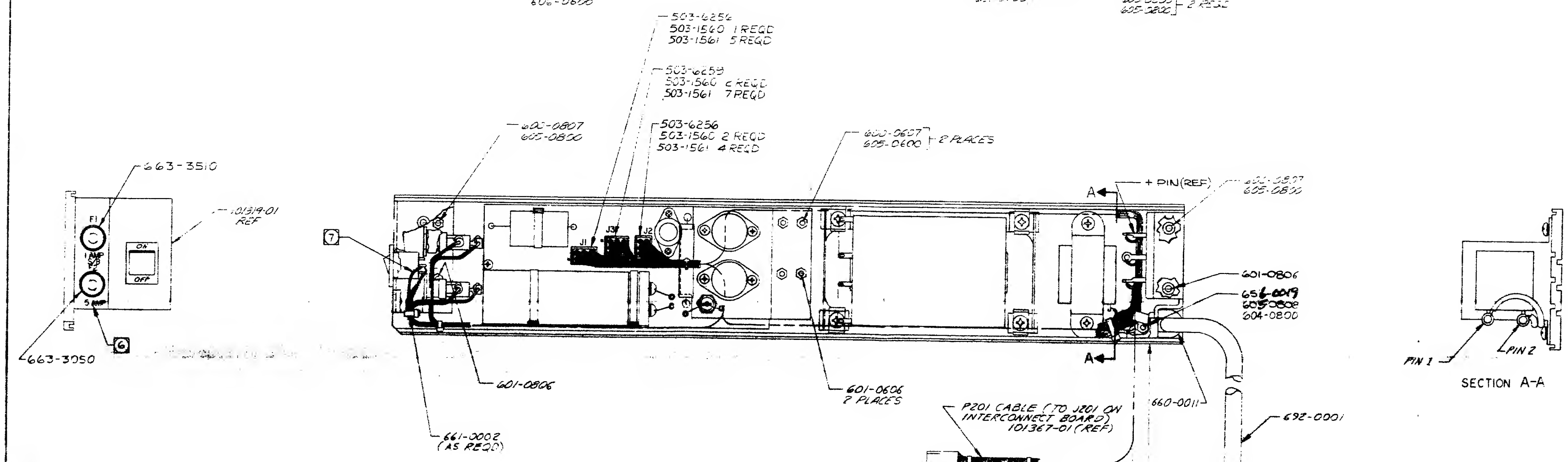
REV	DESCRIPTION	DATE	DR	CHK	APPR
B	ERN 2-SR				
C	ECN 2394				
D	ECN 2551				
E	ECN 2891A				

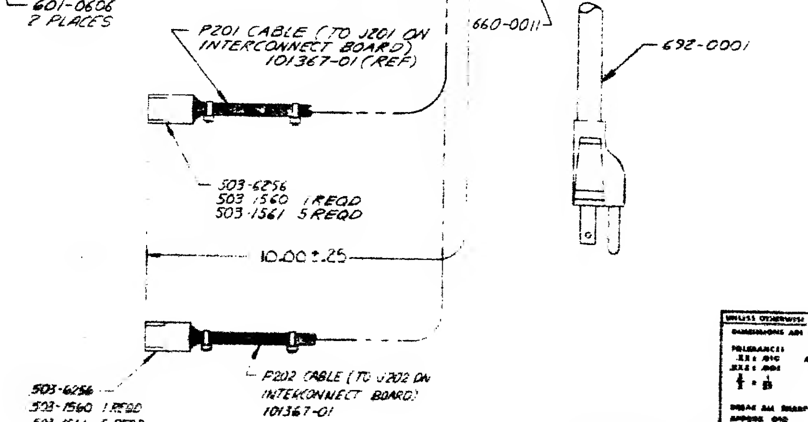
(8) TABLE I

TERMINAL CONNECTORS FOR LINE VOLTAGE VARIATIONS		
LINE VOLTS	LINE INPUT	CONNECT
100	2 AND 3	2 TO 6 AND 3 TO 7
115	2 AND 4	2 TO 6 AND 4 TO 8
125	1 AND 4	1 TO 5 AND 4 TO 8
200	2 AND 7	3 TO 6
210	1 AND 7	3 TO 6
220	1 AND 7	3 TO 5
230	2 AND 8	4 TO 6
240	1 AND 8	4 TO 6
250	1 AND 8	4 TO 5









8. FOR TRANSFORMER PRIMARY CONNECTIONS SEE TABLE I (115 V SHOWN)

7. SHRINK TUBING ON ALL TERMINALS AS REQUIRED

6. RUBBER STAMP WITH NON SMEARABLE INK, 1/8 HIGH CHARACTERS APPROX AS SHOWN.

5. ALL SCREWS TO BE TORQUED AS FOLLOWS: NO.4 TO 6 IN.LBS NO.6 TO 11 IN.LBS, NO.8 TO [illegible] IN.LBS, NO.10 TO [illegible] IN.LBS.

4. FOR LIST OF MATERIALS SEE 101814-01

3. ASSEMBLE PER STANDARD MFG. METHODS.

2. APPLY (665-0001 SILICONE GREASE) BETWEEN HEATSINK OF 101336-01 (101945) AND CHASSIS (101811) AS SHOWN.

1. RUBBER STAMP ASSY NO. 101814-01 IN LEGIBLE SIZE CHARACTERS.

NOTES UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
.XX ± .010
.XXX ± .005
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS
APPROX .010

NEXT ASSY	USED ON
101813	1600

APPLICATION

FINISH

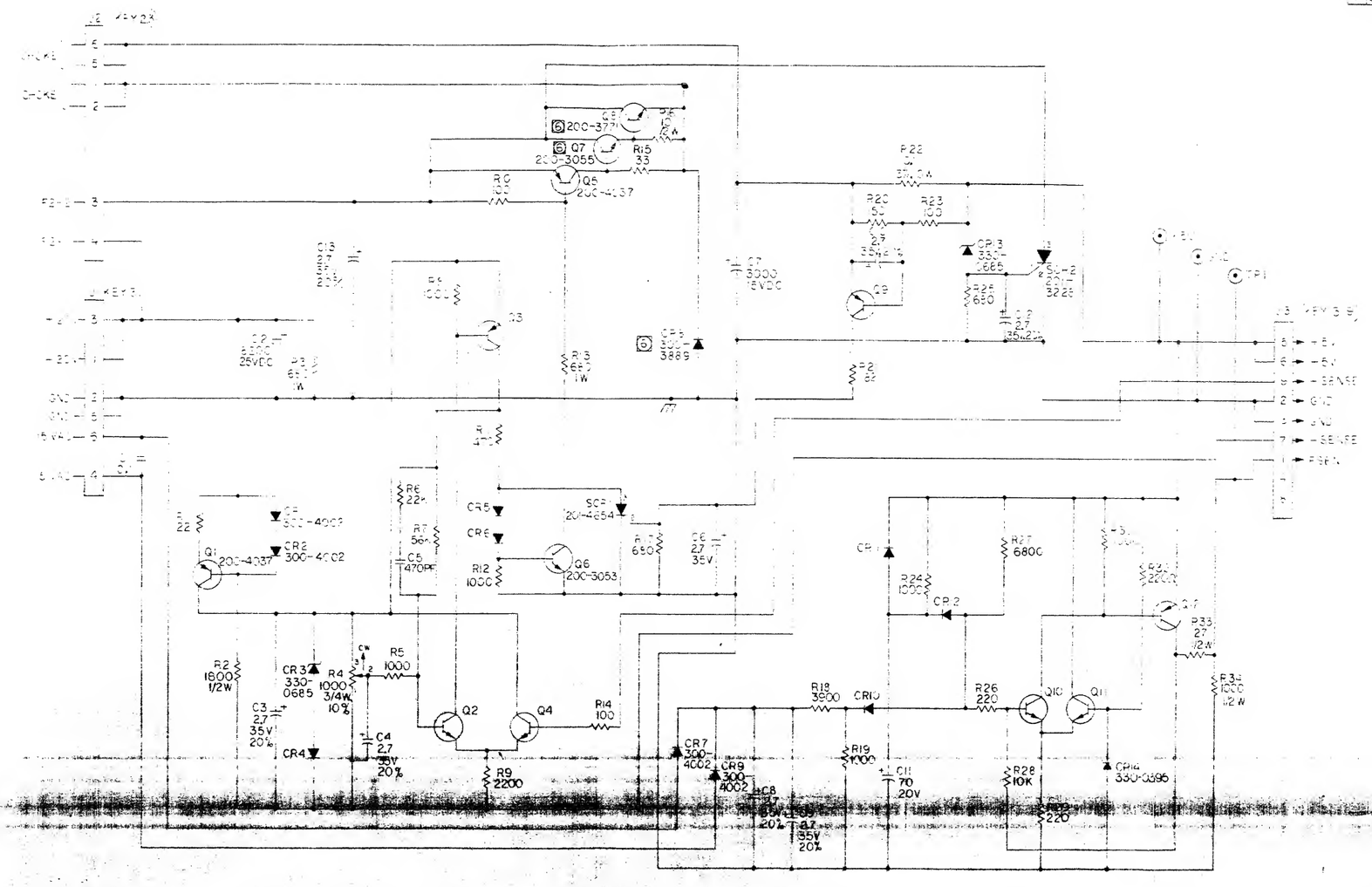
MATL

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE POWER SUPPLY ASSY

SIZE E DWG NO. 101813 REV F

REVISIONS				
REV	DESCRIPTION	DATE	DR	CHK
B	ECN 2077			
C	ECN 2225			
D	ECN 2327			
E	ECN 2348			
F	ECN 2485			
G	ECN 2799A			
H	ECN 2951			
J	ECN 3042			
K	ECN 3046A			



(6) INDICATES COMPONENTS MOUNTED ON HEATSINK.
4. FOR ASSEMBLY DRAWING SEE 101336.
3. FOR SPECIFICATION DRAWING SEE 101339.
2. ALL NPN TRANSISTORS ARE PEC 200-4123.
ALL PNP TRANSISTORS ARE PEC 200-4125.
3. ALL CAPACITORS IN MICROFARADS, 100V, 10%.
2. ALL DIODES ARE PEC 300-4446.
1. ALL RESISTORS IN OHMS, 1/4W, 5%.
NOTES: UNLESS OTHERWISE SPECIFIED:

REFERENCE DESIGNATIONS	
LAST USED	DELETED
R34	R31
C 4	C14
CR14	
SCR2	
Q12	
TP1	

PEC PERIPHERAL EQUIPMENT CORPORATION

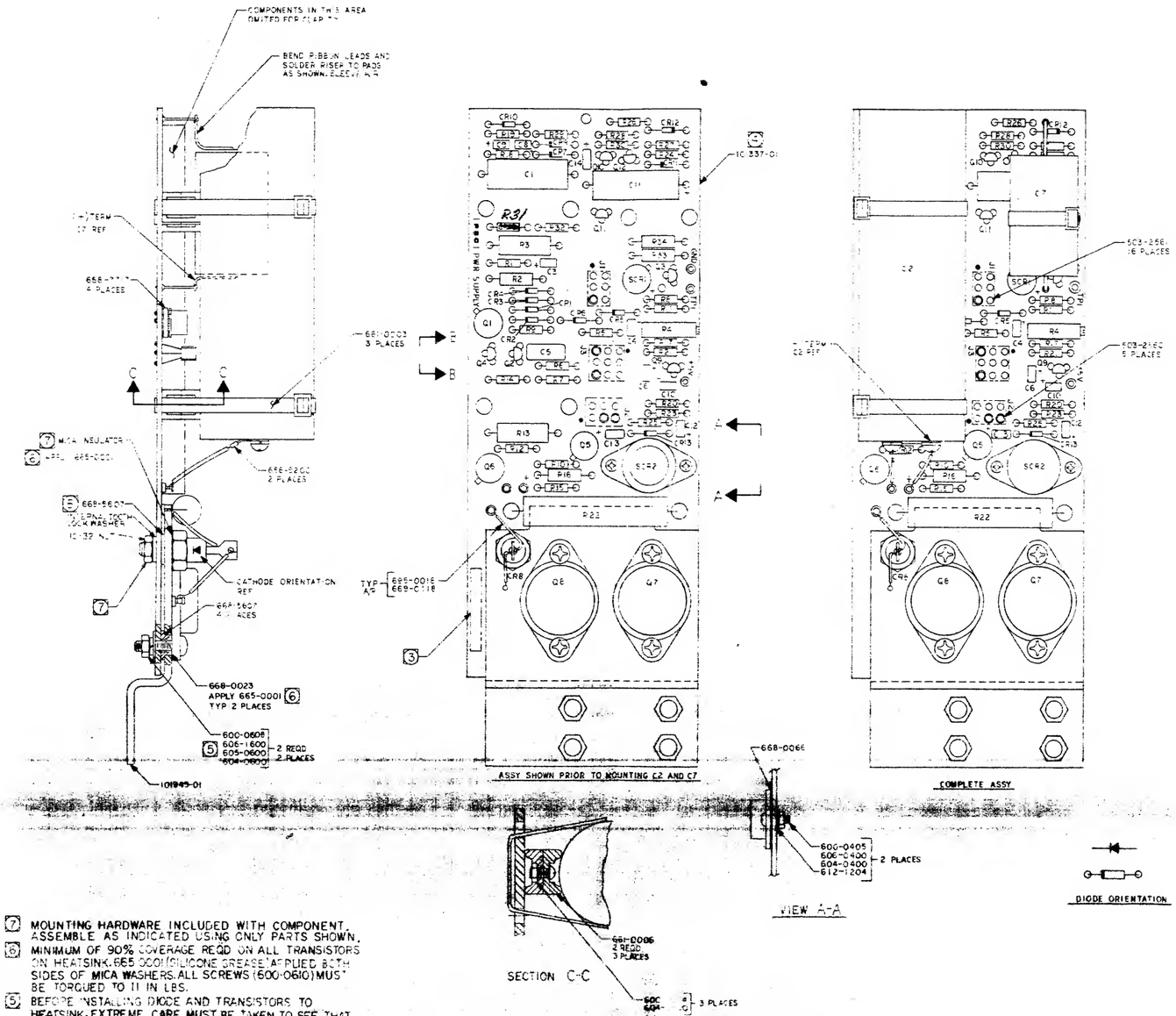
TITLE SCHEMATIC — POWER SUPPLY P.C.B.

SIZE E | 101335 | REV K

8 7 6 5 4 3 2 1

H G F E D C B A

REVISIONS				
REV	DESCRIPTION	DATE	BY	CHK	APPD
C	ECN 2-TY				
D	ECN 2006				
E	ECN 2032				
F	ECN 2107				
G	ECN 2343				
H	ECN 2453				
J	ECN 2779A				
K	ECN 2957				
L	ECN 3295				
M	ECN 3446A				



PART NO.	REF DESIG.
100-1015	R10,14,23
100-1025	R5,8,12,30
	R19,24
100-1035	R28
100-1515	R20
100-2205	R1
100-2215	R29,26,32
100-2225	R9
100-3925	R18
100-6815	R17,27
100-6825	R27
100-4715	R11
100-3305	R15
100-6805	R21
101-1025	R34
101-1005	R16
101-1825	R2
101-2705	R33
102-6815	R3,13
110-0011	R22
100-2235	R6
100-5635	R7
121-1020	R4
130-4715	C5
131-1040	C1
134-8000	C2

PART NO.	REF DESIG.
132-2752	C3,4,6,8, 9,10,12,13
133-7060	C11
134-3000	C7
200-3053	Q6
200-3055	Q7
200-3771	Q8
200-4037	Q1,5
200-4123	Q2,4,10,11
200-4125	Q3,9,12
201-3226	SCR2
201-4654	SCR1
300-3889	CR8
300-4002	CR1,2,7,9
300-4044	CR4,5,6,10,12
330-0685	CR3,13
330-0395	CR16

7. MOUNTING HARDWARE INCLUDED WITH COMPONENT. ASSEMBLE AS INDICATED USING ONLY PARTS SHOWN.
6. MINIMUM OF 90% COVERAGE REQD ON ALL TRANSISTORS ON HEATSINK. 665-0001 SILICONE GREASE APPLIED BOTH SIDES OF MICA WASHERS. ALL SCREWS (600-0610) MUST BE TORQUED TO 11 IN LBS.
5. BEFORE INSTALLING DIODE AND TRANSISTORS TO HEATSINK, EXTREME CARE MUST BE TAKEN TO SEE THAT ALL BURRS AND MISC CHIPS OF METAL ARE WIPED OFF ENTIRE MOUNTING SURFACE.
4. THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101337-01 REV D.
3. RUBBER STAMP ASSY PART NO. INCLUDING VERSION NO. AND ISSUE LETTER.
2. ASSEMBLE PER STANDARD MANUFACTURING METHODS.
1. REF DRAWINGS: SCHEMATIC - 101335
SPECIFICATION - 101339

NOTES, UNLESS OTHERWISE SPECIFIED:

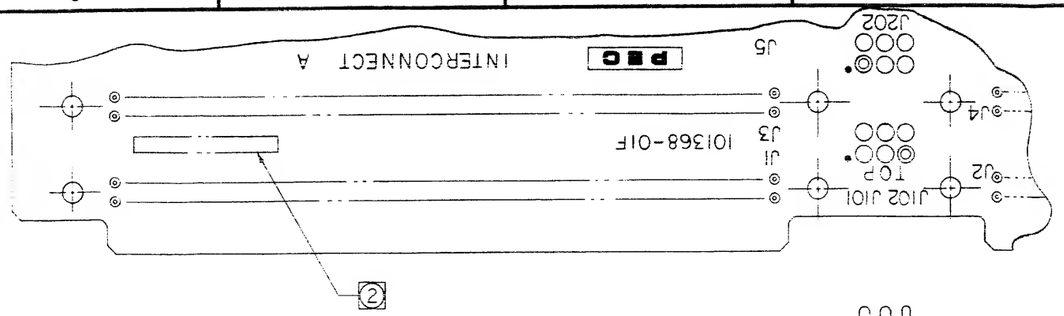
PED PERIPHERAL EQUIPMENT DEVELOPMENT CORPORATION

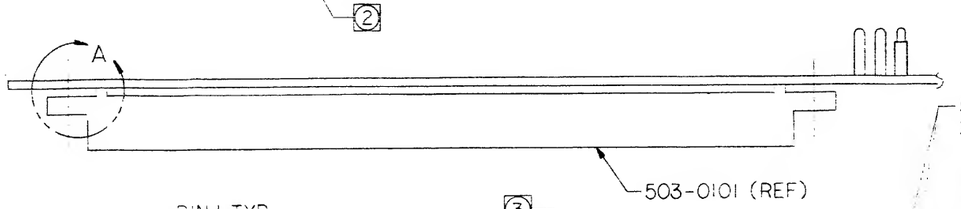
TITLE PCBA POWER SUPPLY

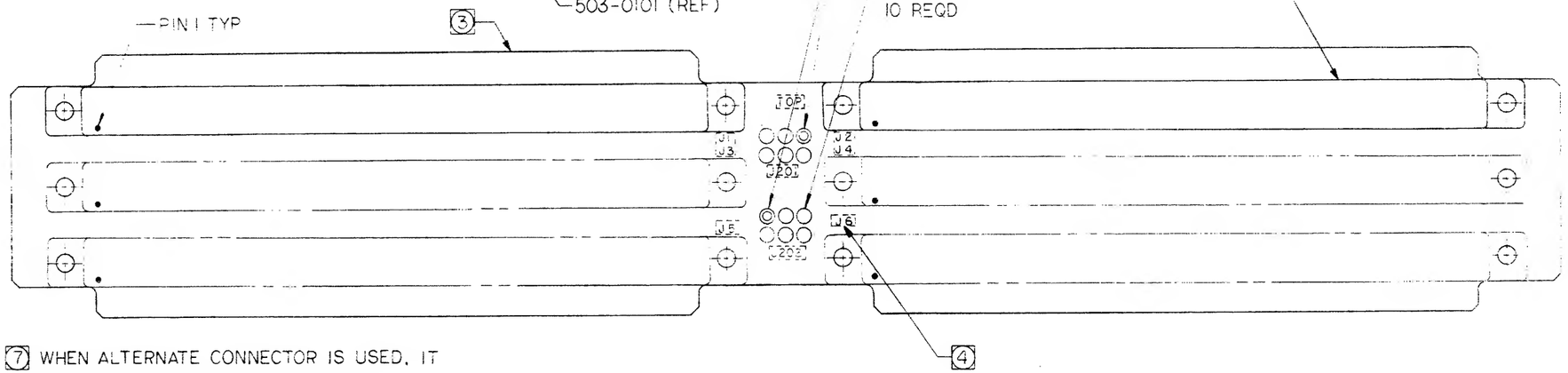
SIZE E | DWG NO 101336 | REV L

SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN2-SJ	7/17/74	JK	KTF	
B	ECN 1935B	10-3-74	TB	CJK	
C	ECN 2314A	2-25-77			
D	ECN 2458	10-24-77			
E	ECN 2437	12-27-77			
F	ECN 2700	12-27-78			PA
G	ECN 3000	9/10/79	PAS		A
H	ECN 3158	11/2/82	PAS		A







COMPONENT SIDE
-01 SHOWN

7 WHEN ALTERNATE CONNECTOR IS USED, IT MUST BE USED IN ALL CONNECTOR POSITIONS ON APPLICABLE DASH NO.

6 WHEN ASSEMBLING BOTH THE -01 AND -02 VERSIONS, MASK REMAINING CONNECTOR MOUNTING HOLES BEFORE WAVE SOLDERING.

5. (DELETED)

4 LETTERING AND REF DESIGNATIONS INDICATED [ ] APPROX AS SHOWN ON FAR SIDE OF BOARD.

3 THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101368 REV G AND SUBSEQUENT.

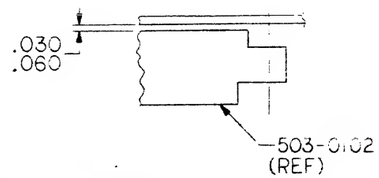
2 RUBBER STAMP PART NO., INCLUDING VERSION NO. AND ISSUE LETTER.

1. ASSEMBLE PER STANDARD MFG METHODS.

NOTES: UNLESS OTHERWISE SPECIFIED

6

CONNECTOR TABLE		
DASH NO.	CONN QTY	CONNECTOR POSITION
-01	2	J1 & J2
-02	4	J1,2,5 & 6
-03	6	J1 THRU J6



DETAIL A
(ALTERNATE CONDITION)

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
.XX ± .010 ANGULAR ± ½°
.XXX ± .005
X ± 1/64
BREAK ALL SHARP CORNERS APPROX. .010
FINISH
MATL:

THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE

SIGNATURES	DATE
DR	7/17/74
CHK	7/17/74
DES	
ENGR	
ENGR	

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE P.C.B.A. INTERCONNECT A

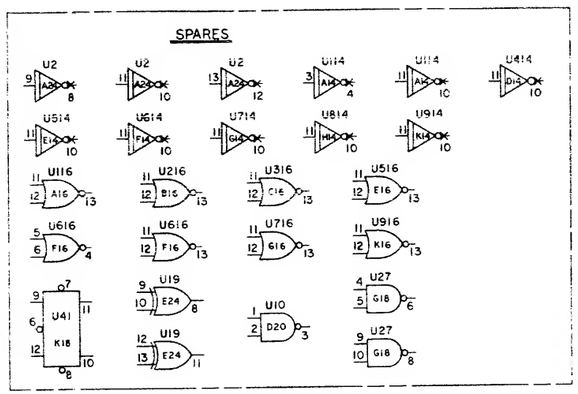
TOP ASSY	1600
NEXT ASSY	1ST USED ON
APPLICATION	

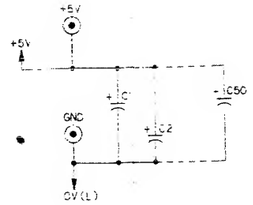
SIZE D | CODE IDENT NO. | DWG NO. 101367 | REV H

SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1

REVISIONS				
REV	DESCRIPTION	DATE	DR	CHK APPR
A	ERN 3-CA			
B	ECN 2640			

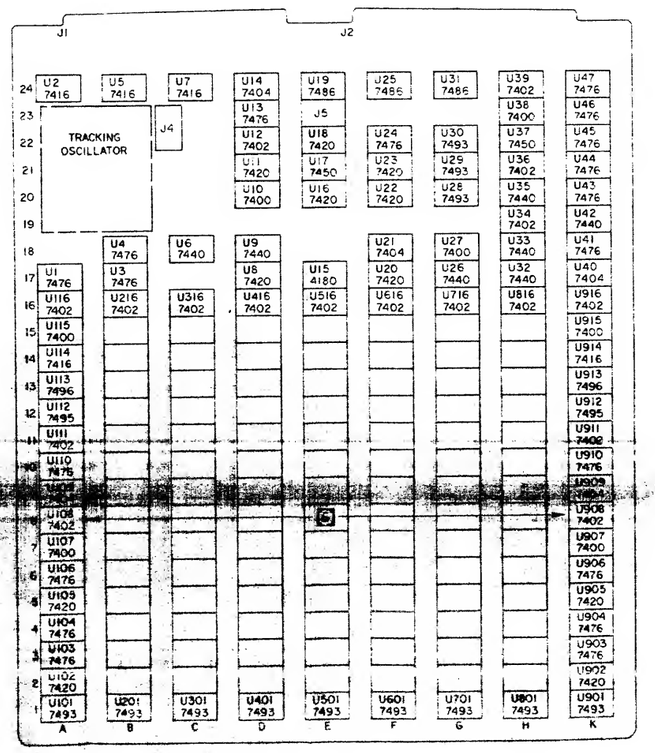
SPARES





GROUND AND POWER PIN NUMBERS

INTEGRATED CIRCUITS	GND	+5V
7400, 7402, 7404, 7416, 7420, 7440, 7450, 7486, 7495, 4180	7	14
7476	13	5
7493	10	5
7496	12	5



REFERENCE DESIGNATION		
LAST USED		DELETED
U47	U916	
R34		
C50		
TP14	TP209	

TABLE I

[9]	INTERNAL INTERFACE RESISTORS	TRANSPORT INTERFACE RESISTORS
VERSION	R1, R4 THRU R12	R15, R16, R18 THRU R33
-01	USE	USE
-02	USE	OMIT
-03	OMIT	USE

[9] SEE VERSION TABLE FOR USAGE.

8. ▷ * DENOTES OPEN COLLECTOR OUTPUT.

7. INTERNAL LABEL (D16) DENOTES COORDINATE LOCATION ON ASSY.

[6] CIRCUIT 100 IS TYPICAL OF CIRCUITS 200 THRU 900.
CIRCUIT 100 IS CHANNEL 0, LOCATION A1 THRU A16.
CIRCUIT 200 IS CHANNEL 0, LOCATION B1 THRU B16.
CIRCUITS 300 THRU 900 ARE CHANNELS 1 THRU 7 RESPECTIVELY, LOCATION C1 THRU C16 ON THRU K1 THRU K16.

5. 3 DIGIT REFERENCE DESIGNATIONS ARE ASSIGNED TO REPETITIVE CIRCUITS. EX: U101 IS CIRCUIT 100. U901 IS CIRCUIT 900. SINGLE DIGIT REFERENCE DESIGNATIONS ARE ASSIGNED TO NON-REPETITIVE CIRCUITS. EX: U1, U2.

4. ALL INTEGRATED CIRCUITS ARE PEC PART NO. PREFIX 700-.

3. ALL RESISTORS ARE 1/4W, ±5%, VALUES ARE IN OHMS.

2. ALL CAPACITORS ARE 2.7UF, 35V, ±20%.

1. REFERENCE DRAWINGS: ASSEMBLY - 101381
SPECIFICATION - 101384

NOTES: UNLESS OTHERWISE SPECIFIED:

8	7	6	5	4	3	2	1	

PEC PERIPHERAL EQUIPMENT CORPORATION

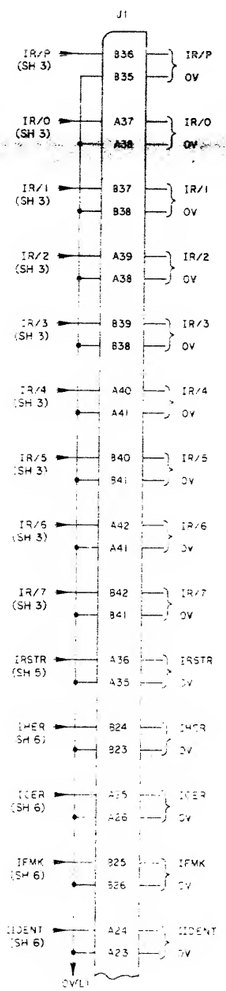
TITLE SCHEMATIC (PCBA)
READ 1600 CPI
PE FORMATTER

SIZE	DWG NO.	REV
E	101380	B

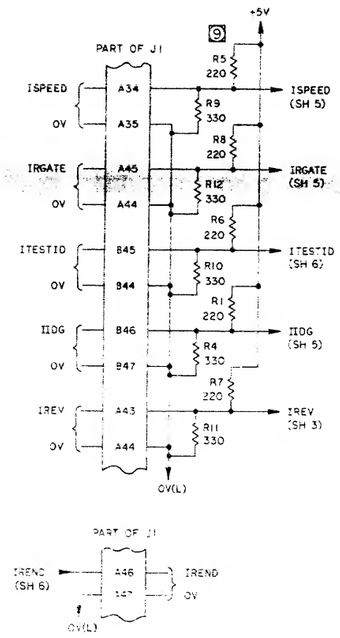
101381	1600
APPLICATION	

REVISIONS				
REV	DESCRIPTION	ECO#	BY	CHK'D APP'D
	SEE SHEET 1			

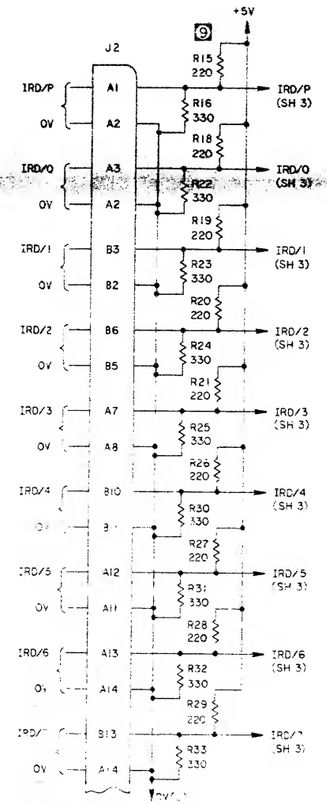
FORMATTER TO CONTROLLER



INTERNAL

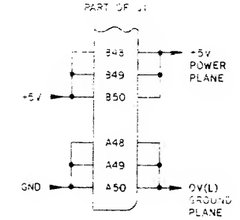


TRANSPORT TO FORMATTER



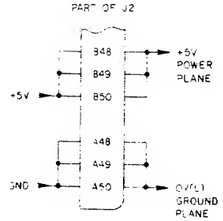
POWER

FROM POWER SUPPLY CONNECTOR J3 (1,2,3,4) VIA MOTHER BOARD



POWER

FROM POWER SUPPLY CONNECTOR J3 (1,2,3,4) VIA MOTHER BOARD



UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
X.X ± .010 ANGULAR ± 1°
XXX ± .005
X ± 1
X ± 1/1
✓
BREAK ALL SHARP CORNERS APPROX .010

THE INFORMATION HEREON IS THE PROPRIETARY PROPERTY OF PEC AND IS LOANED SUBJECT TO AGREEMENT THAT IT WILL NOT BE REPRODUCED OR COPIED IN WHOLE OR IN PART NOR USED IN ANY MANNER DETRIMENTAL TO THE INTEREST OF PEC

SIGNATURES	DATE
DR	7/14/77
CHK	7/14/77
ENGR	
ENGR	

FINISH: MATL:

NEXT ASSY | 1ST USED ON | APPLICATION

INTERFACE

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA)
READ 1600 CPI
PE FORMATTER

SIZE E | DWG NO. 101380 | REV B

SCALE | DO NOT SCALE PRINT | SHEET 2 OF 5

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				

SEE SHEET 4 FOR TYPICAL CIRCUIT

TP101 — IRD/P J2-A1 — U19 F24 — RD/P — CIRCUIT 100 (CHANNEL P) — DATA/P — U5 A2 — TP201 — IR/P J1-B36

TP102 — IRD/0 J2-A3 — U25 F24 — RD/0 — CIRCUIT 200 (CHANNEL 0) — DATA/0 — U7 K2 — TP202 — IR/0 J1-A37

TP103 — IRD/1 J2-B3 — U25 F24 — RD/1 — CIRCUIT 300 (CHANNEL 1) — DATA/1 — U7 K2 — TP203 — IR/1 J1-B37

TP104 — IRD/2 J2-B6 — U25 F24 — RD/2 — CIRCUIT 400 (CHANNEL 2) — DATA/2 — U7 K2 — TP204 — IR/2 J1-A39

TP105 — IRD/3 J2-A7 — U25 F24 — RD/3 — CIRCUIT 500 (CHANNEL 3) — DATA/3 — U7 K2 — TP205 — IR/3 J1-B39

TP106 — IRD/4 J2-B10 — U31 G24 — RD/4 — CIRCUIT 600 (CHANNEL 4) — DATA/4 — U7 K2 — TP206 — IR/4 J1-A40

TP107 — IRD/5 J2-A12 — U31 G24 — RD/5 — CIRCUIT 700 (CHANNEL 5) — DATA/5 — U2 A2 — TP207 — IR/5 J1-B40

TP108 — IRD/6 J2-A13 — U31 G24 — RD/6 — CIRCUIT 800 (CHANNEL 6) — DATA/6 — U2 A2 — TP208 — IR/6 J1-A42

TP109 — IRD/7 J2-B13 — U31 G24 — RD/7 — CIRCUIT 900 (CHANNEL 7) — DATA/7 — U2 A2 — TP209 — IR/7 J1-B42

+5V — R17 1K — TP12 — IREV J1-A43 — U14 — U19 E24 — REV

MONITOR SOCKET U5 E23

13	NDROP/P (SH 4)
2	NDROP/0
1	NDROP/1
14	NDROP/2
15	NDROP/3
9	NDROP/4
7	NDROP/5
10	NDROP/6
11	NDROP/7 (SH 4)
3	NERR1 (SH 6)
4	NERR2 (SH 6)
5	NERR3 (SH 6)
6	NERR4 (SH 6)
12	RGATE1 (SH 5)
16	+5V
8	0V (L)

(SH 4) DA/C, /1, /2, /3, /4, /5, /6, /7 — PARITY GENERATOR U15 E17 — TP9 — PE (SH 6)

DA/P (SH 4) — U21

+5V — R4 470 — NDROP/P (SH 4) — U2 B16 — U1 B16 — NDROP/0 (SH 4) — U2 B15 — U1 B15 — U2 B16 — U3 C16 — NDROP/1 (SH 4) — U3 E15 — U3 C15 — U3 E16 — U4 D16 — NDROP/2 (SH 4) — U4 E15 — U4 D15 — U4 E16 — U5 F16 — NDROP/3 (SH 4) — U5 E15 — U5 F15 — U5 E16 — U6 F16 — U6 F14 — NDROPDET2 (SH 6) — U6 F15 — DROPDET1 (SH 6)

NDROP/4 (SH 4) — U7 G16 — U7 G14 — NDROP/5 (SH 4) — U7 G15 — U7 G16 — U8 H16 — U8 H14 — NDROP/6 (SH 4) — U8 H15 — U8 H16 — U9 K16 — U9 K14 — NDROP/7 (SH 4) — U9 K15 — U9 K16

+5V — R13 470 — (SH 4) CHDET/P, /0, /1, /2, /3, /4, /5, /6 — CHDET/7 (SH 4) — CHDET (SH 6)

+5V — R34 470 — (SH 4) POSTDET/P, /0, /1, /2, /3, /4, /5, /6 — POSTDET/7 (SH 4) — POSTDET (SH 6)

+5V — R3 470 — (SH 4) NONEDET/P, /0, /1, /2, /3, /4, /5, /6 — NONEDET/7 (SH 4) — NONEDET (SH 6)

+5V — R2 470 — (SH 4) NBODET/P, /0, /1, /2, /3, /4, /5, /6 — NBODET/7 (SH 4) — NBODET (SH 6)

COMBINED CHANNEL LOGIC

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA) READ 1600 CPI PE FORMATTER

SIZE E — DWG NO 101360 — REV G

REVISIONS				
REV	DESCRIPTION	DATE	DR	CHK	APPD
	SEE SHEET 1				

PARC (SH 6)

PRESET (SH 6)

CIRCUIT 100 (6) (CHANNEL P)

SLCLK

SRCLK

SHL

NCOPYA (SH 5)

NRCLK (SH 5)

U107 A7

U111 A11

U111 A11

CONTROL

U112 A12

NECLK (SH 5)

OV(L)

U114 A14

CHDET/RQ,1 THRU 7 (SH 3)

RD/P D1 THRU 7 (SH 3)

U104 A4

U105 A5

U107 A7

U106 A6

U102 A2

U108 A8

U109 A1

RD1

RD2

NRD1

DSTR

BUFFER

SYNC

U110 D2 A10

DATA/RQ1 THRU 7 (SH 3)

PARC

U115 A15

U116 A16

U117 A17

CHDET/RQ,1 THRU 7 (SH 3)

NCHDET/RQ,1 THRU 7 (SH 3)

NRQDET/RQ,1 THRU 7 (SH 3)

DSTR-SYNC

RGATE1 (CHANNEL P, 1 & 2) RGATE2 (CHANNEL 2, 3 & 4) RGATE3 (CHANNEL 5,6 & 7) (SH 5)

U103 A3

REN2 (SH 6)

NDP

REN2

DGATE

NDGATE

DGATE/0 & 2 (CKT 200 & 400 ONLY) (SH 5)

DROP

NDROP

DROP/RQ0,1 THRU 7 (SH 3)

J5 (SH 3)

RCLK1 (CHANNEL P) RCLK2 (CHANNEL 0 & 1) RCLK3 (CHANNEL 2 & 3) RCLK4 (CHANNEL 4 & 5) RCLK5 (CHANNEL 6 & 7) (SH 5)

DSTR

ENV

ENV/2 (SH 5) ENV/RQ4,5,6,7 (SH 6) (CKT 100,200,400, 700,800 & 900 ONLY)

NENV/0,2 (SH 5) NENV/1,3 (SH 6) (CKT 200 THRU 600 ONLY)

REN1 (SH 6)

INDIVIDUAL CHANNEL LOGIC

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES: XX ± .010 ANGULAR; XXX ± .005 ± ½°; X ± .03 ✓. BREAK ALL SHARP CORNERS APPROX .010	SIGNATURES	DATE	PEC PERIPHERAL EQUIPMENT CORPORATION	
	DR		TITLE SCHEMATIC (PCBA) READ 1600 CPI PE FORMATTER	
	CHK			
	ENGR			
	MFGR			
NEXT ASSY	FINISH	MATL	SIZE E	DWG NO. 101330	REV B
APPLICATION			SCALE	DO NOT SCALE DWG	SHEET 3 OF 8

8 7 6 5 4 3 2 1

H G F E D C B A

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				

TRACKING OSCILLATOR U4

CLOCK
+5V
NER2
NER1
OV(L)

U40 U40 U40 U40 U40 U40 → U32 H17 → NECLK (SH 4)

U5 K18 → RCLK1 (CHANNEL P) (SH 4)
U9 D18 → RCLK2 (CHANNEL 0 & 1) (SH 4)
U9 D18 → RCLK3 (CHANNEL 2 & 3) (SH 4)
U33 H18 → RCLK4 (CHANNEL 4 & 5) (SH 4)
U33 H18 → RCLK5 (CHANNEL 6 & 7) (SH 4)
U6 K18 → RCLK6 (CONTROL) (SH 6)
NPCLK (SH 4 & 6.
U26 G17 → RGATE1 (CHANNEL P,0 & 1) (SH 3,4 & 6)
U26 G17 → RGATE2 (CHANNEL 2,3 & 4) (SH4 & 6)
U32 H17 → (SH 4) RGATE3 (CHANNEL 5,6 & 7)
NRGATE (SH 6)

TP1
DATA2
U1 A17, U1 A17, U3 B17, U3 B17, U4 B18
ER1 → U314 C18 → 10
ER2 → U214 B18 → 10
OV(L)

TP10
ISPEED J1-A34
U14 SPEED

RCLK6

(SH 4) DGATE/2
(SH 4) ENV/2
(SH 4) DGATE/0
NENV/2 (SH 4)
U17 E21 → TRACKSIG
U116 A16
U4 B18
U115 A15

TP13
IRGATE J1-A45
U14 RGATE
U816 H16

TP7
IIDG J1-B46
U14 IDG
U14 NIDG
U27 G18 → NLO (SH 4)

NRCN: (SH 6)
U21 F16
U27 G18 → NDATA
NENV/0 (SH 4)
U21 F16 → DATA1

(S/FE) (SH 6)
CHDET (SH 3)
U21 F16
U34 H19
CCN2
RCLK6
U46 K23
U47 K24
CCN1
U38 H23
NCOPYP
U24 H24
U39
OVCL
NCOPY
U47 K24
NCCN2

(RCN4·NRCN5) (SH 6)
U35 H20 → COPY (SH 6)
NCOPYA (SH 4)
U34 H19
NRCLK
COPYCLK (SH 6)

RCTR5
(SH 6) RCN4
(SH 6) NRCN2
RCTR6
RCTR5
RCTR1
RCTR0
RCTR4
U23 F21
U34 H19
U22 F20
U23 F21
U22 F20
TP14
U24 F22
RP (SH 6)
NRP (SH 6)

CCN2
RCLK6
RP
RCTR0 RCTR1 RCTR2 RCTR3 → U28 G20
RCTR4 RCTR5 RCTR6 RCTR7 → U29 G21
RCTR8 RCTR9 RCTR10 RCTR11 → U30 G22

U21 F16
NRP
NRCN7
NDATA
U17 E21
U18 F22
RCN7 (SH 6)
(SH 6) NRCN7
(S/RCN7) (SH 6)
U38 H23
U34 H19
RSTR
U5 B06
TP6
RSTR (SH 6)
IRSTR J1-A36
NCCN2 (SH 6)
NDATA (SH 6)
DATA1 (SH 6)

READ CONTROL LOGIC

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA) READ 1600 CPI PE FORMATTER

SIZE E | DWG NO 101380 | REV D

NEXT ASSY | USED ON | APPLICATION

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
	SEE SHEET 1				

(SH 3) POSTDET
COPYCLK (SH 5)
(SH 5) RCLK6 (CONTROL)
(SH 5) NRCLK
NRP (SH 5)
NDATA (SH 5)
NRGATE (SH 5)
RGATE1 (SH 5)
NDROPDET2 (SH 3)
(SH 3) NONEDET
(SH 3) NBODET
COPY (SH 5)
(SH 5) NCCN2
RP (SH 5)
DATA1 (SH 5)

NRCN1
NRCN2
RPCLK
RCN2
RCN3
RCN5
RCN6
RCN7
RCLK6
RGATE1
REND
NRP
OV(L)
NTESTONES
FE
NCCN2
NERR3
NERR2
NERR4
RP

NRCN1 (SH 5)
NRCN2 (SH 5)
RCN4 (SH 5)
(S/RCN7) (SH 5)
NRCN7 (SH 5)
IREND J1-A46
RCN7 (SH 5)
PRESET (SH 4)
(S/FE) (SH 5)
NERR1, J5-3 (SH 3)
NERR2, J5-4 (SH 3)
NERR3, J5-5 (SH 3)
NERR4, J5-6 (SH 3)

NRCN6
RCN6
(RCN4·NRCN5)
RCN5
NRCN4
NRCN5
RCN2
REN1 (SH 4)
REN2 (SH 4)
IFMX J1-B25
(RCN4·NRCN5) (SH 5)
IHER J1-B24

(SH 4) ENW5
(SH 4) ENW0
(SH 4) ENW3
(SH 4) ENW7
(SH 4) ENW6
(SH 4) ENW2
(SH 4) NENW4
(SH 4) NENW3
(SH 4) NENW1
(S/FM)
FM
NRCN1
RPCLK
NFE
HE

COPYCLK
PE (SH 3)
DROPDET1 (SH 3)
(SH 5) RGATE2
RSTR (SH 5)
TESTID J1-B46
TESTID
CORRECT
IDENT
IDENT J1-A24
PARC (SH 4)
IOER J1-A25

U36 H21 U39 H24 U38 H23 U46 K23 U41 K18 U7 C24 TP8
U43 K20 U44 K21 U45 K22 U37 H22 U12 D22 U18 E22 U24 F22 U16 E20
U42 K19 U35 H20 U5 B20 TP5 TP3 TP2 TP4
U8 D17 U10 D20 U13 D23 U20 F17 U21 U11 D21 U14 D16 U4,5

READ CONTROL & ERROR LOGIC

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: X.X ± .010 X.XX ± .005 ANGS. ± ½° ½ ± 1/64
BREAK ALL SHARP CORNERS APPROX. .010
FINISH:

SIGNATURES	DATE
DR	
CHK	
APPR	
ENGR	
MGR	

MATL:

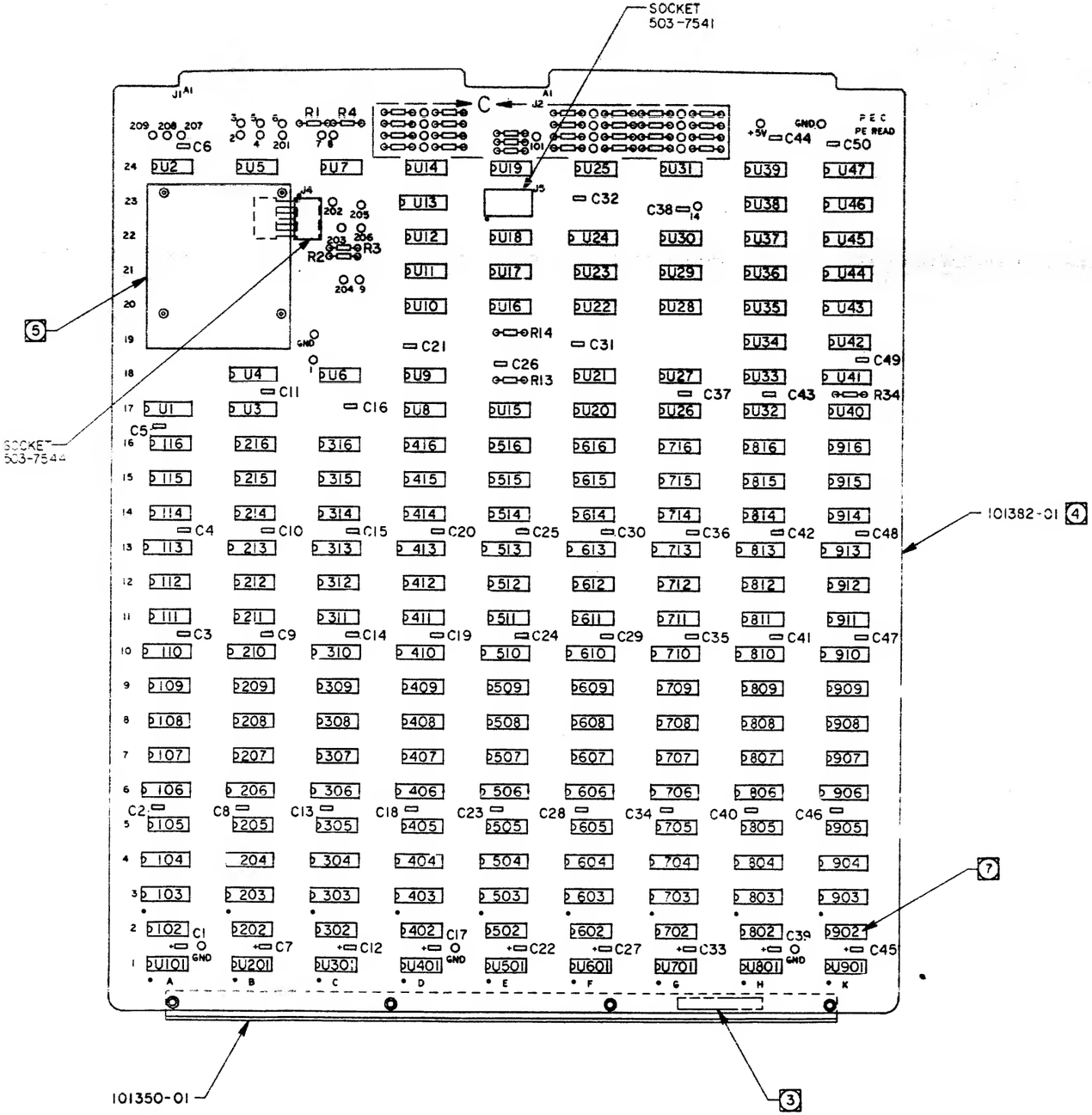
PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA) READ 1600 CPI PE FORMATTER

NEXT ASSY | USED ON | APPLICATION

SIZE E | DWG NO 101380 | REV B | SCALE | DO NOT SCALE DRWG | SHEET 6 OF 9

8 7 6 5 4 3 2 1
H G F E D C B A



7 DESIGNATION U, IS INTENTIONALY OMITED ON SOME ICS FOR CLARITY.

6 FOR PARTS AFFECTED BY VERSION NO. SEE TABLE II.

5 SEE TOP BILL FOR CORRECT VERSION OF TRACKING OSCILLATOR.

4 THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101382-01 REV E AND SUBSEQUENT.

3 RUBBER STAMP ASSY PART NO. INCLUDING VERSION AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MFG METHODS.

1. REFERENCE DRAWINGS: SCHEMATIC-101380
SPECIFICATION-IC1384

NOTES: UNLESS OTHERWISE SPECIFIED:

615-4703
4 REQD
MFG HD
THIS SIDE

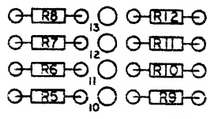
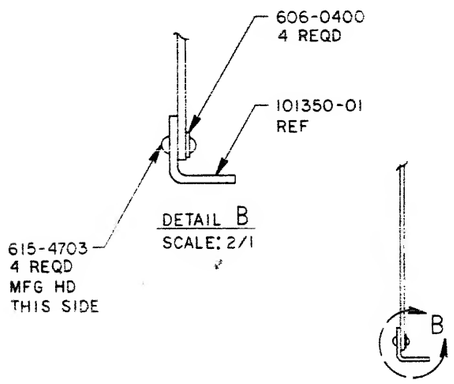


TABLE I

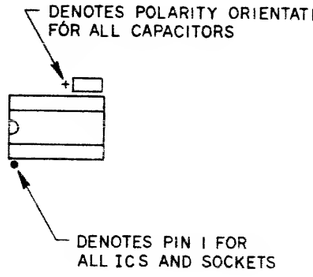
PART NUMBER	REFERENCE DESIGNATION
100-1025	R17
100-2215	R1, 5-8, 15, 18-21, 26-29
100-3315	R4, 9-12, 16, 22-25, 30-33
100-4715	R2, 3, 13, 14, 34
132-2752	C1-50
700-4180	U15
700-7400	U10, 27, 38, 107-907, 115-915
700-7402	U12, 34, 36, 39, 108-908, 111-911, 116-916
700-7404	U14, 21, 40, 109-909
700-7416	U2, 5, 7, 114-914
700-7420	U8, 11, 16, 18, 20, 22, 23, 102-902, 105-905
700-7440	U6, 9, 26, 32, 33, 35, 42
700-7450	U17, 37
700-7476	U1, 3, 4, 13, 24, 41, 43-47, 103-903, 104-904, 106-906, 110-910
700-7486	U19, 25, 31
700-7493	U28, 29, 30, 101-901
700-7495	U112-912
700-7496	U113-913

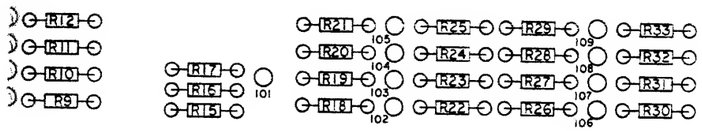
6	INTERN
VERSION	RI
-01	
-02	
-03	

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APVD
B	ERN 3-CA	4/23/71	[illegible]	[illegible]	[illegible]
C	ECN 2496	4/27/71	[illegible]	[illegible]	[illegible]
D	ECN 2538A	4/27/71	[illegible]	[illegible]	[illegible]
E	ECN 2539	4/27/71	[illegible]	[illegible]	[illegible]
F	ECN 2635	5/24/71	[illegible]	7/12/71	[illegible]



DETAIL B
SCALE: 2/1

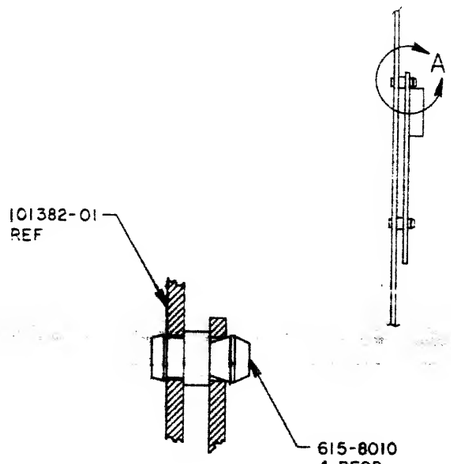




DETAIL C
SCALE: 2/1

TABLE II

6	INTERNAL INTERFACE RESISTORS	TRANSPORT INTERFACE RESISTORS
VERSION	R1, R4 THRU R12	R15, R16, R18 THRU R33
-01	USE	USE
-02	USE	OMIT
-03	OMIT	USE



DETAIL A
SCALE: 4/1
INSTALL IN
DIRECTION
SHOWN

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR ± ½°
.XXX ± .005
X ± 1/64
X ± 1/32
BREAK ALL SHARP CORNERS
APPROX. .010

THE INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE

SIGNATURES	DATE
DR [illegible]	4/26/71
CHK [illegible]	4/26/71
ENGR [illegible]	4/27/71

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE
PCBA —
READ 1600 CPI
PE FORMATTER

TOP ASSY 1600
NEXT ASSY
APPLICATION

FINISH:
MATL:

SIZE E
DWG NO. 101381
REV F
SCALE 1/1
DO NOT SCALE DRWG
SHEET
OF

6

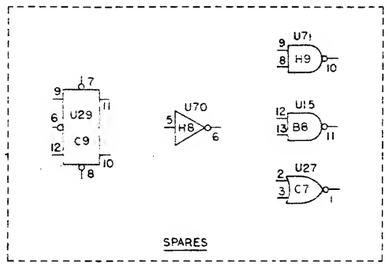
REVISIONS					
REV	DESCRIPTION	DATE	BY	CHK	APPD
A	ERN 3-BC	9/11	[illegible]	[illegible]	[illegible]
B	ECN 2599	5/12	[illegible]	[illegible]	[illegible]
C	ECN 2651	9/12	[illegible]	[illegible]	[illegible]

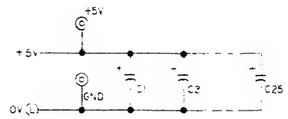
VERSION TABLE (7)

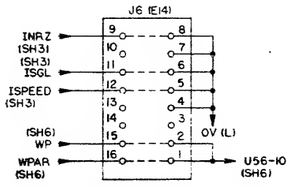
DASH NO	U19,20,31,32,41-44, U54-57,59-61,63, U65-67,70-73	R1-48	R51-68	W1,2	DESCRIPTION
-01	USE	USE	USE	OMIT	NORMAL
-02	USE	OMIT	USE	OMIT	OMIT CONTROLLER INTERFACE TERMINATOR
-03	USE	OMIT	OMIT	OMIT	OMIT CONTROLLER AND TRANSPORT INTERFACE TERMINATORS
-04	OMIT	USE	USE	USE	READ ONLY

GROUND AND POWER PIN NUMBERS

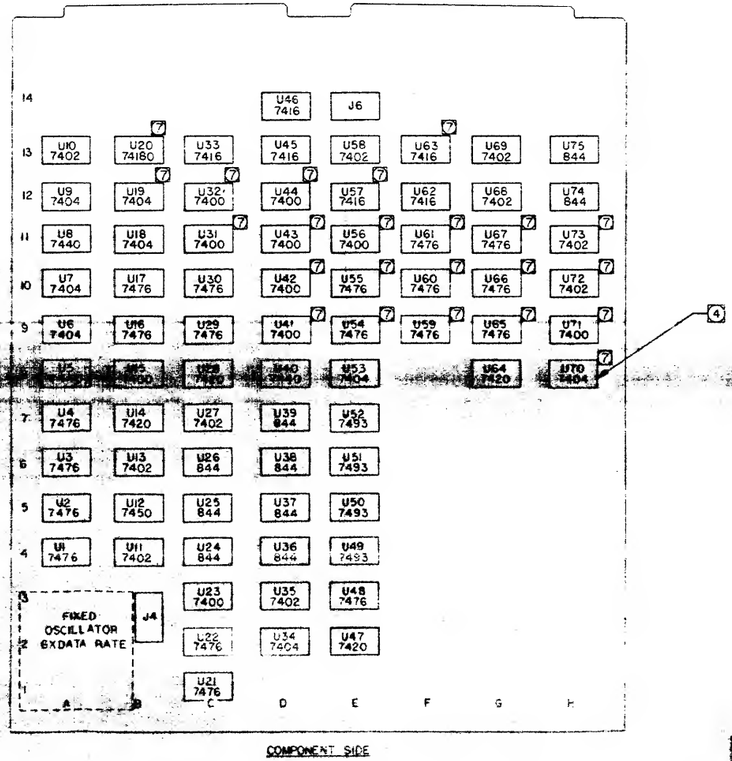
INTEGRATED CIRCUITS	GND	+5V
700-7400,7402,7404,7416, 7420,7440,7450, 74180,8440	7	14
700-7476	13	5
700-7493	10	5





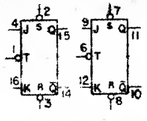


JUMPER PLATFORM
SEE ASSY DWG NO 102100, 102101, 102102 & 102103.



COMPONENT SIDE

REFERENCE DESIGNATION	
LAST USED	DELETED
R74	
C26	
U75	
TP109	
TP209	
TP21	



8. ALL FLIP FLOPS USED FUNCTIONALY AS FOLLOWS:
7. SEE VERSION TABLE FOR USAGE.
6. ⊸ DENOTES OPEN COLLECTOR OUTPUT.
5. INTERNAL LABEL (C2) DENOTES COORDINATE LOCATION ON ASSY.
4. ALL INTEGRATED CIRCUITS ARE PEC PART NO. PREFIX 700-.
3. ALL CAPACITORS ARE 2.7UF, 100V, 10%.
2. ALL RESISTORS ARE 1/4W, 5%, VALUES ARE IN OHMS.
1. REFERENCE DRAWINGS: ASSEMBLY-101386
SPECIFICATION -101389

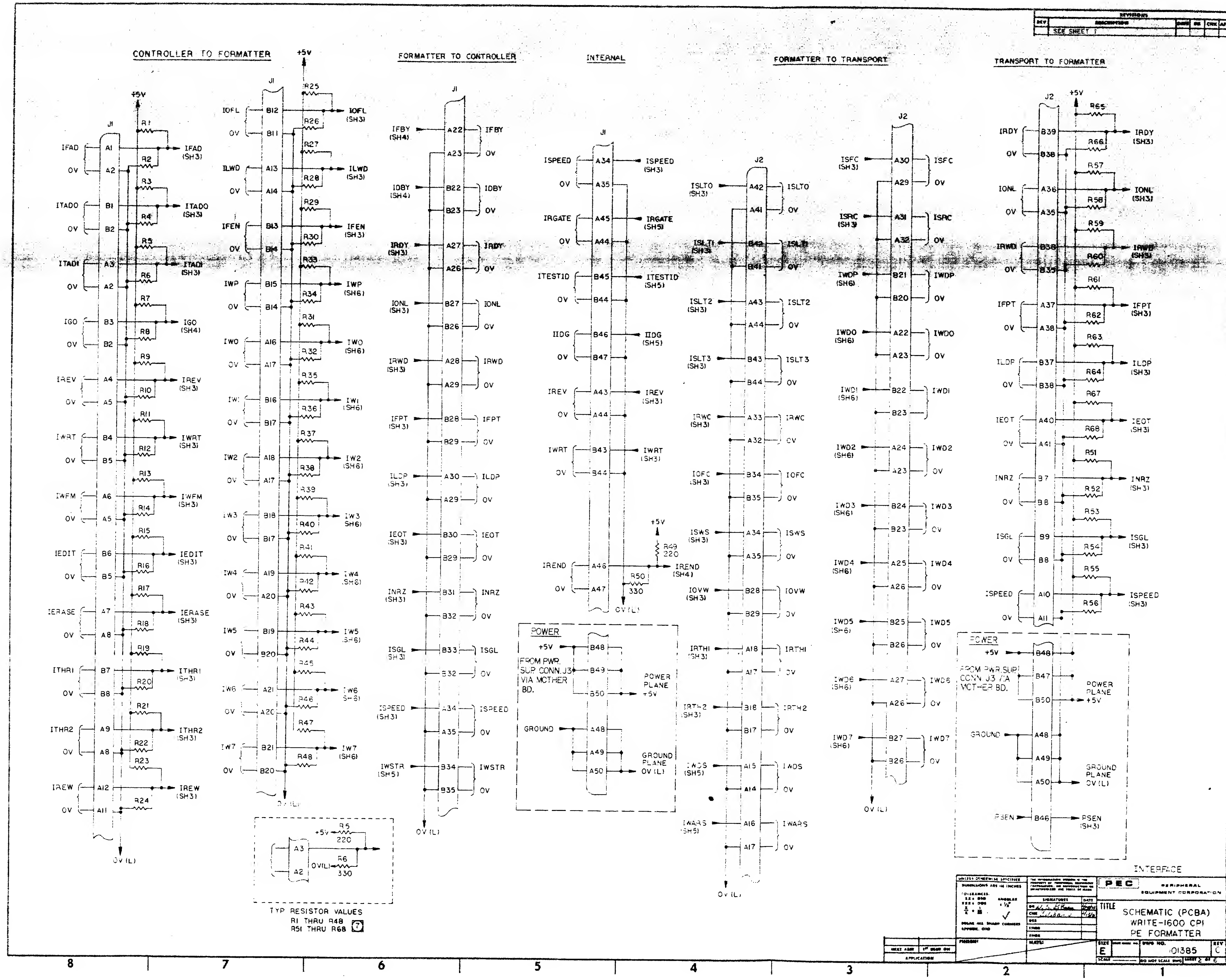
NOTES: UNLESS OTHERWISE SPECIFIED:

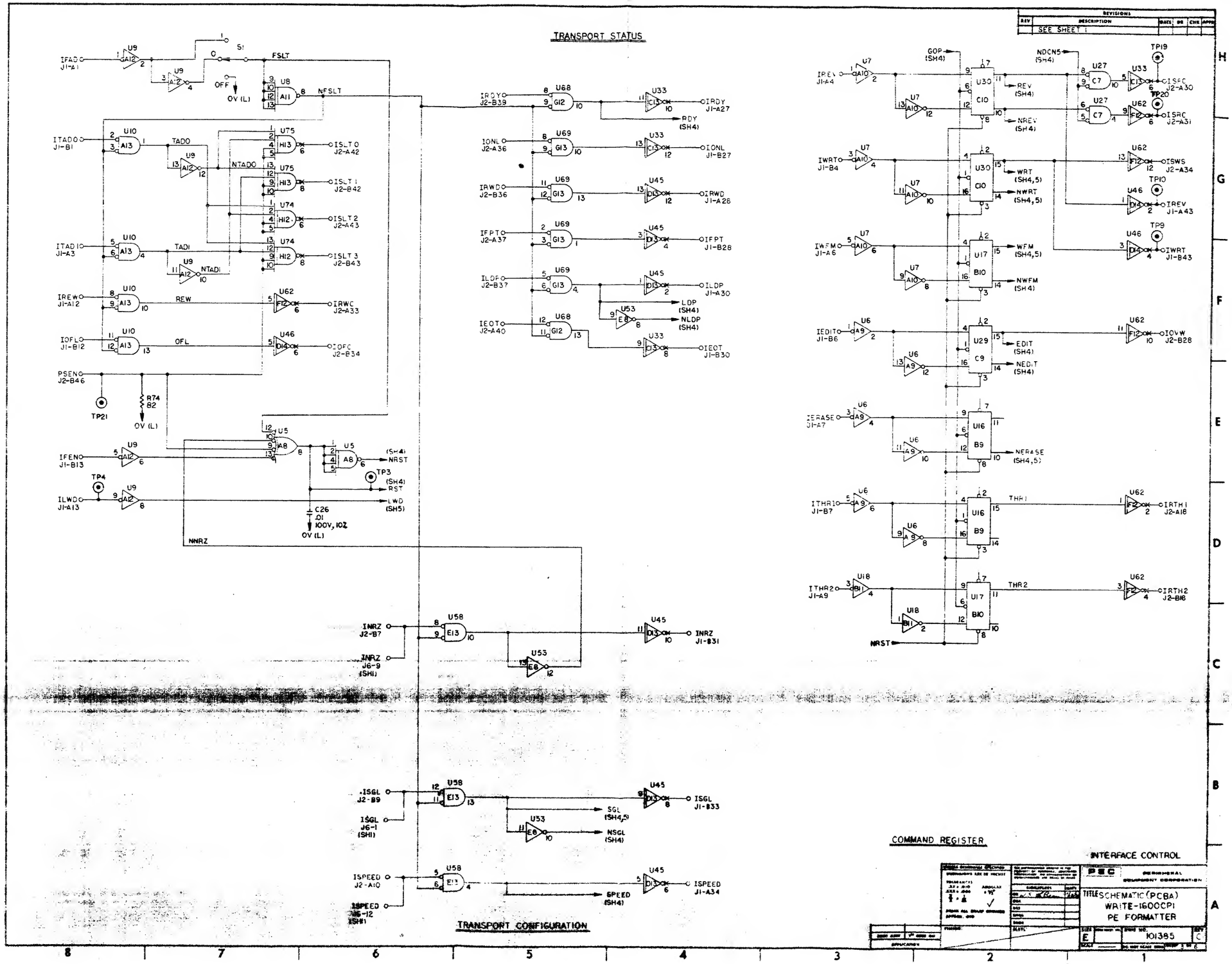
PEC PERIPHERAL EQUIPMENT CORPORATION

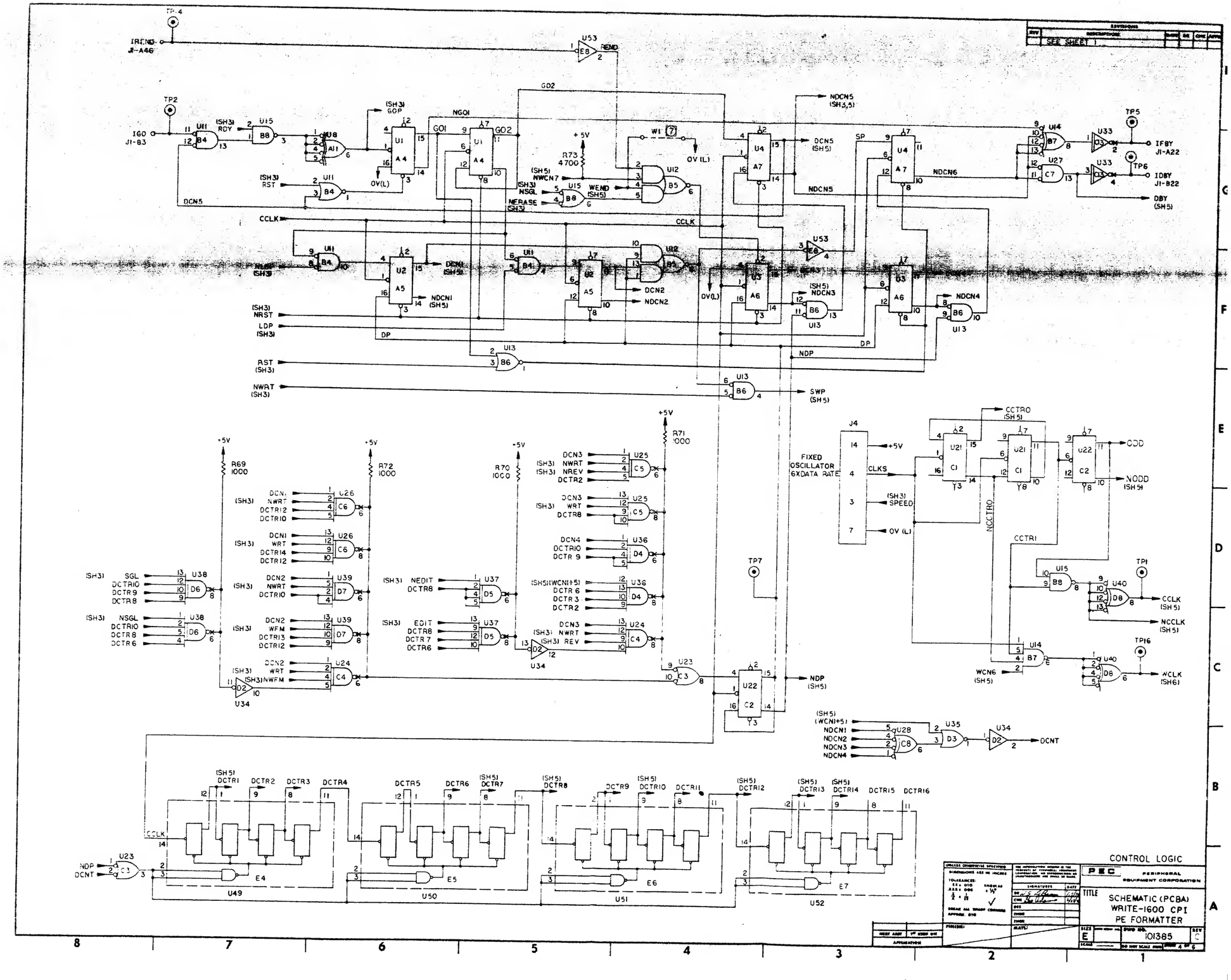
TITLE SCHEMATIC (PCBA) WRITE-1600 CPI PE FORMATTER

SIZE E | DWG NO 101385 | REV C

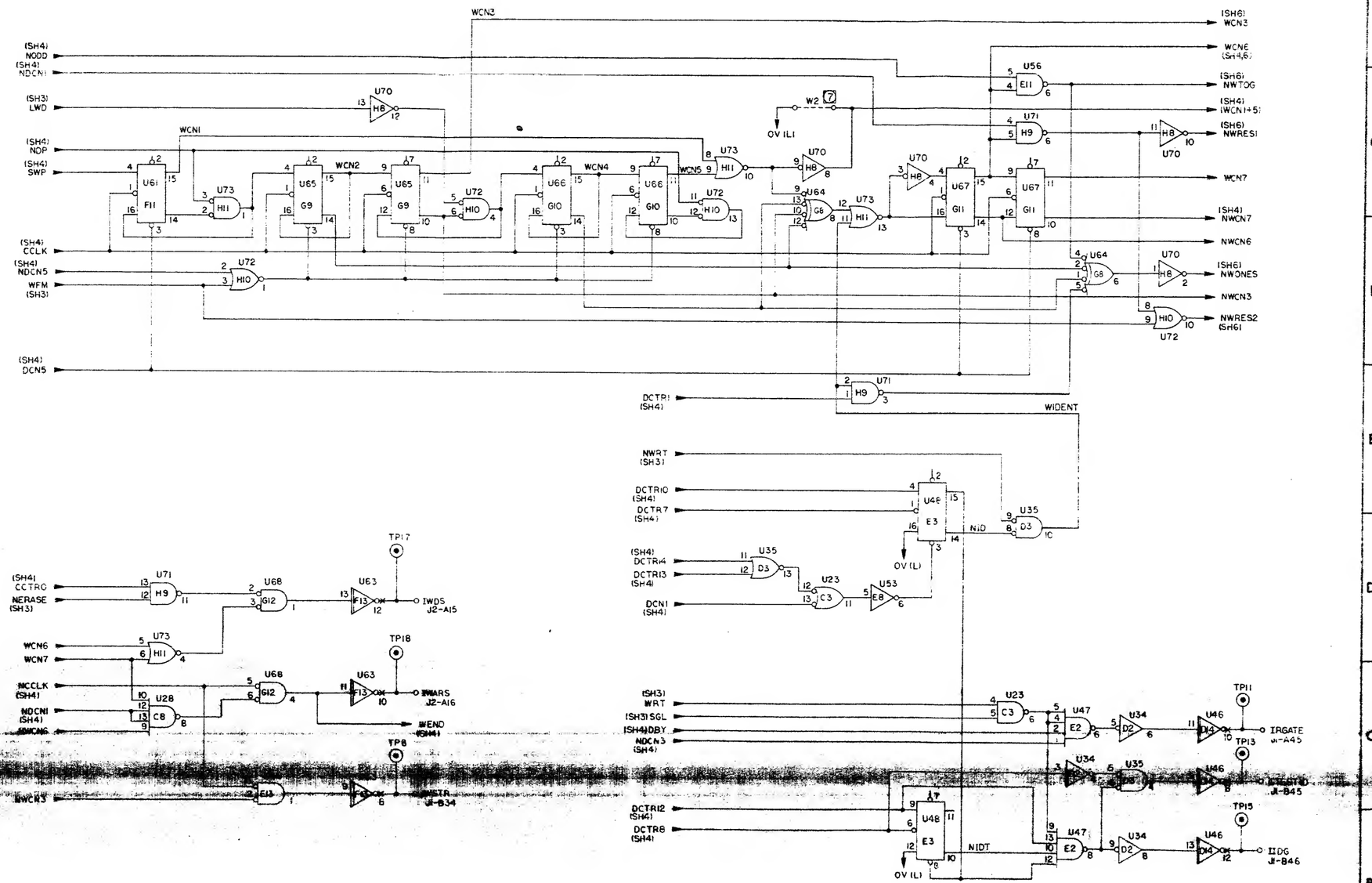
DO NOT SCALE DRAWING | SHT 1 OF 1


CONTROLLER TO FORMATTER
FORMATTER TO CONTROLLER
INTERNAL
FORMATTER TO TRANSPORT
TRANSPORT TO FORMATTER
SEE SHEET 1
POWER
FROM PWR. SUP. CONN. J3 VIA MOTHER BD.
POWER PLANE +5V
GROUND
GROUND PLANE 0V (L)
TYP RESISTOR VALUES
R1 THRU R48
R51 THRU R68
INTERFACE
PEC
PERIPHERAL EQUIPMENT CORPORATION
TITLE
SCHEMATIC (PCBA)
WRITE-1600 CPI
PE FORMATTER
E
01385
C


REVISIONS
REV DESCRIPTION DATE BY CHK APPD
SEE SHEET 1
TRANSPORT STATUS
IFADO J1-A1
FSLT
NFSLT
OFF
OV (L)
ITADO J1-B1
TADO
NTADO
ISLT 0 J2-A42
ISLT 1 J2-B42
ISLT2 J2-A43
ITADIO J1-A3
TADI
NTADI
ISLT 3 J2-B43
IREW J1-A12
REW
IRWC J2-A33
IOFL J1-B12
OFL
IOFC J2-B34
PSENO J2-B46
TP21
R74 82
IFENO J1-B13
NRST
TP4
TP3
RST
ILWD J1-A13
LWD (SH5)
C26 .01 100V, 10% OV (L)
NNRZ
IRDY J2-B39
RDY (SH4)
IONL J2-A36
IONL J1-B27
IRWD J2-B36
IRWD J1-A26
IFPT J2-A37
IFPT J1-B28
ILOF J2-B37
ILDP J1-A30
LDP (SH4)
NLDP (SH4)
IEOT J2-A40
IEOT J1-B30
INRZ J2-B7
INRZ J1-B31
INRZ J6-9 (SH1)
ISGL J2-B9
ISGL J1-B33
SGL (SH4,5)
NSGL (SH4)
ISGL J6-1 (SH1)
ISPEED J2-A10
ISPEED J1-A34
6SPEED (SH4)
ISPEED J6-12 (SH1)
TRANSPORT CONFIGURATION
GOP (SH4)
NDCNS (SH4)
IPRV J1-A4
REV (SH4)
NREV (SH4)
IWRTO J1-B4
WRT (SH4,5)
NWRT (SH4,5)
IWFM J1-A6
WFM (SH4,5)
NWFM (SH4)
IEDITO J1-B6
EDIT (SH4)
NEDIT (SH4)
IERASE J1-A7
NERASE (SH4,5)
ITHR1O J1-B7
THR1
IRTH1 J2-A18
ITHR2O J1-A9
THR2
IRTH2 J2-B18
NRST
ISWS J2-A34
IRREV J1-A43
IOVW J2-B28
ISRC J2-A30
ISRC J2-A31
IWRT J1-B43
TP19
TP20
TP10
TP9
COMMAND REGISTER
INTERFACE CONTROL
PSC PERIPHERAL STORAGE CORPORATION
TITLE SCHEMATIC (PCBA) WRITE-1600CPI PE FORMATTER
SIZE E
DWG NO. 101385
REV C
SCALE
SHEET 3 OF 6


TP4
IRENO
J1-A46
U53
SEND
TP2
IGO
J1-B3
U11
B4
(SH3)
RDY
U15
B8
U8
A11
U1
A4
(SH3)
GOP
NGOI
GOI
GO2
OV(L)
(SH3)
RST
DCN5
CCLK
+5V
R73
4700
(SH5)
NWCN7
(SH3)
NSGL
U15
B8
WEND
(SH5)
NERASE
(SH3)
WI
7
OV (L)
U12
B5
NDCN5
(SH5,5)
DCN5
(SH5)
SP
U4
A7
NDCN6
NDCN5
U4
B7
U27
C7
U33
Q3
TP5
IFBY
J1-A22
TP6
IDBY
J1-B22
DBY
(SH5)
U2
A5
DCN1
(SH5)
NDCN1
(SH5)
(SH3)
NRST
LDP
(SH3)
DP
RST
(SH3)
NWRT
(SH3)
U13
B6
DCN2
NDCN2
U3
A6
(SH5)
NDCN3
NDCN4
NDP
SWP
(SH5)
+5V
R69
1000
R72
1000
R70
1000
R71
1000
U26
C6
U39
D7
U38
D6
U24
C4
U25
C5
U36
D4
U37
D5
U34
D2
U23
C3
U22
C2
U21
C1
Y3
Y8
J4
14
4
3
7
FIXED
OSCILLATOR
6XDATA RATE
CLKS
(SH3)
SPEED
OV (L)
CCTRO
(SH5)
NCCTRO
CCTRI
ODD
NODD
(SH5)
TP7
TP1
TP16
U15
B8
U40
D8
CCLK
(SH5)
NCCLK
(SH5)
U14
B7
WCN6
(SH5)
WCLK
(SH6)
U28
C8
U35
D3
DCNT
U49
U50
U51
U52
E4
E5
E6
E7
DCTR1
DCTR2
DCTR3
DCTR4
DCTR5
DCTR6
DCTR7
DCTR8
DCTR9
DCTR10
DCTR11
DCTR12
DCTR13
DCTR14
DCTR15
DCTR16
CONTROL LOGIC
PEC
PERIPHERAL
EQUIPMENT CORPORATION
TITLE
SCHEMATIC (PCBA)
WRITE-1600 CPI
PE FORMATTER
SIZE
E
101385
REV
C
SEE SHEET 1

REVISIONS					
REV	DESCRIPTION	DATE	BY	CHK	APPD
	SEE SHEET 1				



WRITE CONTROL

PERIPHERAL EQUIPMENT CORPORATION

TITLE SCHEMATIC (PCBA) WRITE-1600 CPI PE FORMATTER

SIZE E | DWG NO. 101385 | REV C

SCALE | DO NOT SCALE DRAWING | SHT 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	BY	CHK	APPR
	SEE SHEET 1				

PARITY GENERATOR BI3 U20

TP12 WPAR

(SH1) J6-16 (SH1) J6-1

TP101 IWP J1-B15 OV(L) U19 BI2 WP J6-15 (SH1) J6-2 (SH1) U56 E11 U56 E11

TP102 IW0 J1-A16 U18 BI1 W0 U31 C11 U43 D11

TP103 IW1 J1-B16 U19 BI2 W1 U32 C12 U44 D12

TP104 IW2 J1-A18 U19 BI2 W2 U32 C12 U44 D12

TP105 IW3 J1-B18 U18 BI1 W3 U31 C11 U43 D11

TP106 IW4 J1-A19 U18 BI1 W4 U31 C11 U43 D11

TP107 IW5 J1-B19 U18 BI1 W5 U31 C11 U43 D11

TP108 IW6 J1-A21 U19 BI2 W6 U32 C12 U44 D12

TP109 IW7 J1-B21 U19 BI2 W7 U32 C12 U44 D12

U56 E11 U41 D9 U61 F11 U63 F13 TP201 IWDP J2-B21

U42 D10 U60 F10 TP202 IWD0 J2-A22

U41 D9 U59 F9 U57 E12 TP203 IWD1 J2-B22

U41 D9 U54 E9 TP204 IWD2 J2-A24

U42 D10 U55 E10 TP205 IWD3 J2-B24

U42 D10 TP206 IWD4 J2-A25

U41 D9 TP207 IWD5 J2-B25

U42 D10 TP208 IWD6 J2-A27

U41 D9 TP209 IWD7 J2-B27

(SH5)WCN3
(SH5)NWONES
(SH5)NWTOG
(SH4)WCLK
(SH5)NWRES1
(SH5)WCN6
(SH5)NWRES2

WRITE DATA

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
XX ± .010
XXX ± .005
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS APPROX .010

THE INFORMATION CONTAINED IN THIS DRAWING IS THE PROPRIETARY PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION AND IS LOANED SUBJECT TO AGREEMENT THAT NEITHER IT NOR THE INFORMATION CONTAINED THEREIN IS TO BE REPRODUCED, COPIED, LENT OR DISCLOSED IN WHOLE OR IN PART EXCEPT AS SPECIFICALLY AUTHORIZED IN WRITING BY PEC AND THAT IT SHALL BE RETURNED UPON REQUEST.

SIGNATURES DATE
DR 7/21
CHK 7/21
DES
ENGR
ENGR

MATL

NEXT ASSY | USED ON
APPLICATION

PEC PERIPHERAL EQUIPMENT CORPORATION

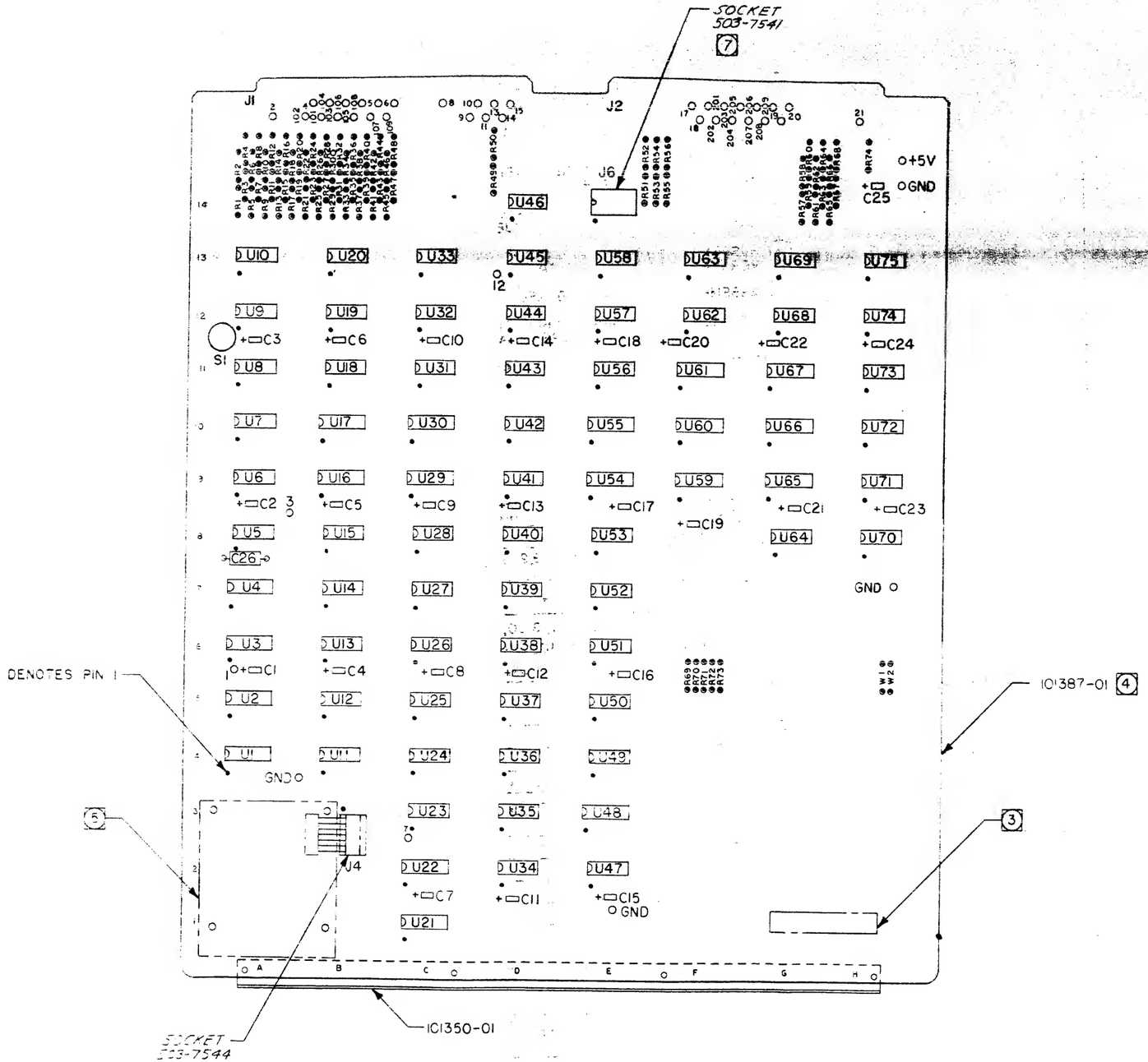
TITLE SCHEMATIC (PCBA)
WRITE-1600CPI
PE FORMATTER

SIZE E | DWG NO. 101385 | REV C

SCALE | DO NOT SCALE DWG | SHEET 6 OF 6

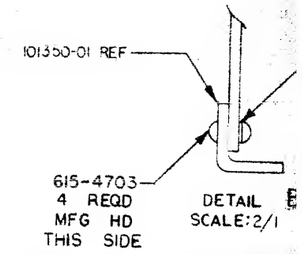
8 7 6 5 4 3 2 1

H G F E D C B A



7. SEE TOP BILL FOR CORRECT VERSION OF 18 PIN DIP JUMPER PLATFORM.
6. FOR PARTS AFFECTED BY VERSION NO. SEE TABLE II.
5. SEE TOP BILL FOR CORRECT VERSION OF FIXED OSCILLATOR.
4. THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101387-01 REV C AND SUBSEQUENT.
3. RUBBER STAMP ASSY PART NO. INCLUDING VERSION AND ISSUE LETTER.
2. ASSEMBLE PER STANDARD MFG METHODS.
1. REFERENCE DRAWINGS: SCHEMATIC-101385
SPECIFICATION-101389.

NOTES: UNLESS OTHERWISE SPECIFIED.



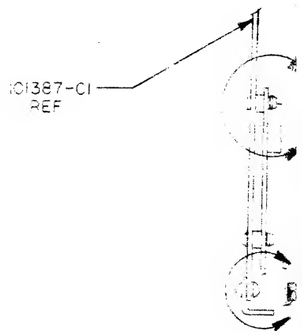


TABLE I

PART NUMBER	REFERENCE DESIGNATION
100-1025	R69-72
100-2215	R1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31, R33,35,37,39,41,43,45,47,49,51,53,55, R57,59,61,63,65,67
100-3315	R2,4,6,8,10,12,14,16,18,20,22,24,26,28, R30,32,34,36,38,40,42,44,46,48,50, R52,54,56,58,60,62,64,66,68
100-4725	R73
100-8205	R74
131-1030	C26
132-2752	C1-25
700-7400	U15,23,31,32,41,42,43,44,56,71
700-7402	U10,11,13,27,35,58,68,69,72,73
700-7404	U6,7,9,18,19,34,53,70
700-7416	U33,45,46,57,62,63
700-7420	U14,28,47,64
700-7440	U5,8,40
700-7450	U12
700-7476	U1,2,3,4,16,17,21,22,29,30,48,54,55,59, U60,61,65,66,67
700-7493	U49,50,51,52
700- 4180	U20
700-8440	U24,25,26,36,37,38,39,74,75
100373-02	W1,2
514-8711	S1

TABLE II

VERSION	U19,20,31,32, U41-44,54-57, U59-61,63, U65-67,70-73	R1-48	R51-68	W1
-01	USED	USED	USED	
-02	USED	NOT USED	USED	
-03	USED	NOT USED	NOT USED	
-04	NOT USED	USED	USED	

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APP'D
B	ERN 3-BC				
C	ECN 2635				

7 SEE TOP BILL FOR CORRECT VERSION OF 16 P.N DIP JUMPER PLATFORM.

6 FOR PARTS AFFECTED BY VERSION NO. SEE TABLE II.

5 SEE TOP BILL FOR CORRECT VERSION OF FIXED OSCILLATOR.

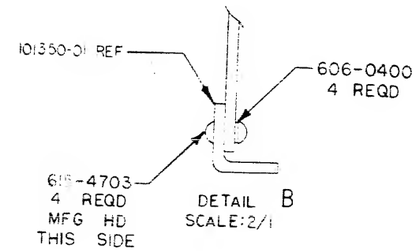
2 THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101387-01 REV C AND SUBSEQUENT.

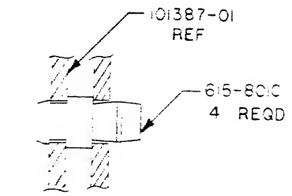
3 RUBBER STAMP ASSY PART NO INCLUDING VERSION AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MFG METHODS.

1. REFERENCE DRAWINGS: SCHEMATIC-101385
SPECIFICATION-101389.

NOTES: UNLESS OTHERWISE SPECIFIED.





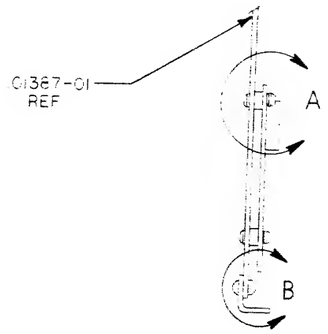


TABLE I

PART NUMBER	REFERENCE DESIGNATION
100-1025	R69-72
100-2215	R1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31, R33,35,37,39,41,43,45,47,49,51,53,55, R57,59,61,63,65,67
100-3315	R2,4,6,8,10,12,14,16,18,20,22,24,26,28, R30,32,34,36,38,40,42,44,46,48,50, R52,54,56,58,60,62,64,66,68
100-4725	R73
100-8205	R74
131-1030	C26
132-2752	C1-25
700-7400	U15,23,31,32,41,42,43,44,56,71
700-7402	U10,11,13,27,35,58,68,69,72,73
700-7404	U6,7,9,18,19,34,53,70
700-7416	U33,45,46,57,62,63
700-7420	U14,28,47,64
700-7440	U5,8,40
700-7450	U12
700-7476	U1,2,3,4,16,17,21,22,29,30,48,54,55,59, U60,61,65,66,67
700-7493	U49,50,51,52
700- 4180	U20
700-8440	U24,25,26,36,37,38,39,74,75
20373-02	W1,2
4-871[illegible]	S1

TABLE II 6

VERSION	U19,20,31,32, U41-44,54-57, U59-61,63, U65-67,70-73	R1-48	~~R51-68~~	W1,2	REMARKS
-01	USED	USED	USED	NOT USED	NORMAL
-02	USED	NOT USED	USED	NOT USED	OMIT CONTROLLER INTERFACE TERMINATORS
-03	USED	NOT USED	NOT USED	NOT USED	OMIT CONTROLLER & TRANSPORT INTERFACE TERMINATORS
-04	NOT USED	USED	USED	USED	OMIT WRITE DATA I.C.'S

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
.XX ± .010 ANGULAR
.XXX ± .005 ± ½°
X ± 1/32
BREAK ALL SHARP CORNERS
APPROX. .010

THIS INFORMATION HEREON IS THE PROPERTY OF PERIPHERAL EQUIPMENT CORPORATION. NO REPRODUCTION OR UNAUTHORIZED USE SHALL BE MADE.

SIGNATURES	DATE
DR	9/6/
CHK	9/6/
DES	
ENGR	9/6/
ENGR	

PEC PERIPHERAL EQUIPMENT CORPORATION

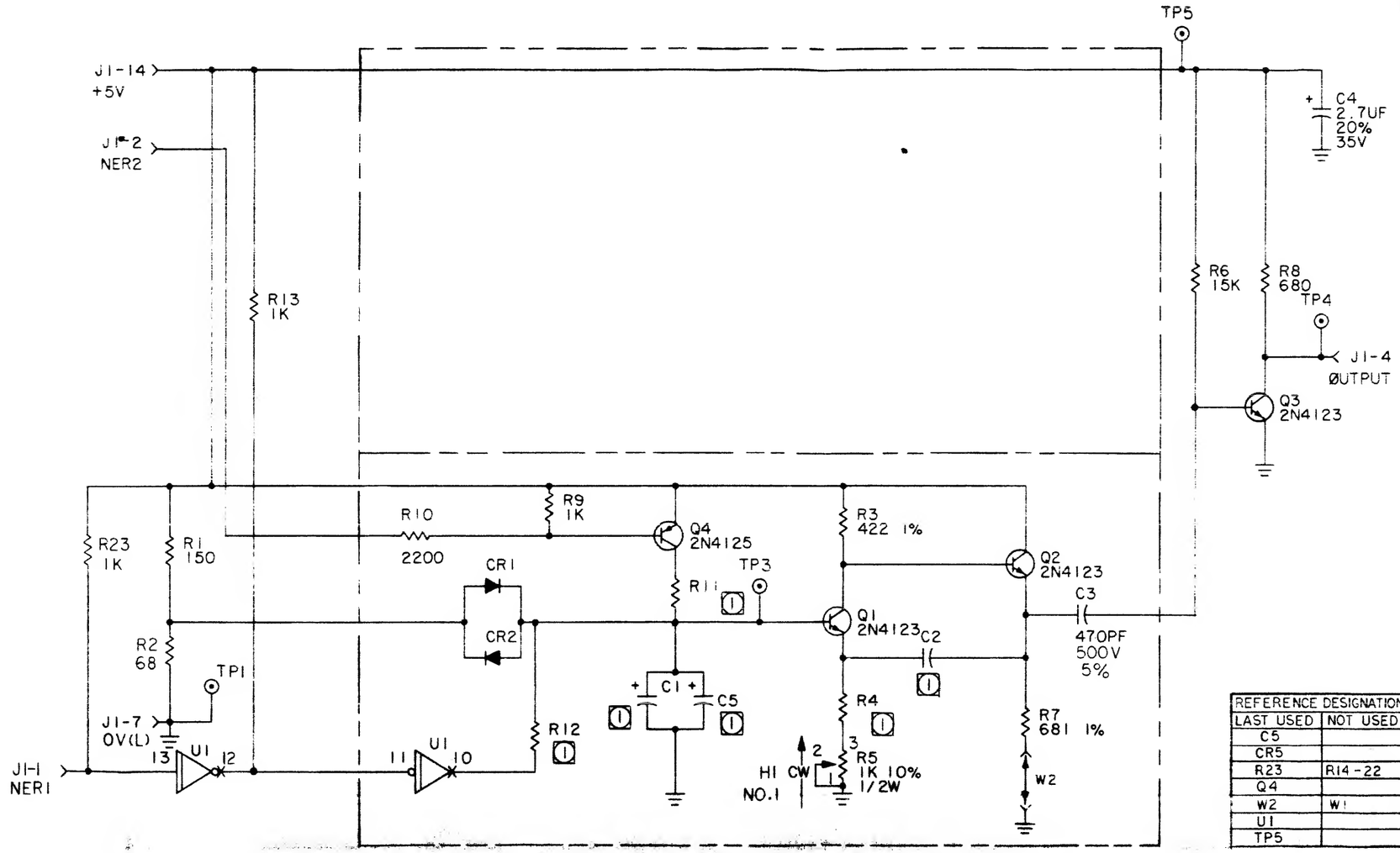
TITLE PCBA
WRITE-1600 CPI
PE FORMATTER

TOP ASSY
NEXT ASSY 1ST USED ON
APPLICATION

FINISH:
MATL:

SIZE E
DWG NO. 101386
REV C
SCALE FULL
DO NOT SCALE DWG
SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 38V	9/1/71	DAE	HG	KJ



REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C5	
CR5	
R23	R14-22
Q4	
W2	W1
U1	
TP5	

[1]

VERSIONS									
DASH NO.	NRZ TAPE SPEEDS (IPS)	R4 (1%)	R11 (1%)	R12 (1%)	C2		C1		C5
					500V, 5%	100V, 10%	35V, 20%	6V, 20%	35V, 20%
-01	31<40	1330	1620	750	330PF	—	2.7UF	—	2.7 UF
-02	24<31	1470	2370	1100	470PF	—	2.7 UF	—	2.7 UF
-03	14.5<22	750	825	383	—	.001UF	—	22UF	—
-04	11<14.5	825	1210	562	—	.0015UF	—	22UF	—
-05	7.5<11	1000	1470	681	—	.0015UF	—	22UF	—
-06	5<7.5	1000	2370	1100	—	.0022UF	—	22UF	—
-07	40<56	909	1470	681	330 PF	—	2.7UF	—	2.7UF
-08	56<90	825	825	383	220PF	—	2.7UF	—	2.7 UF
-09	22<24	1780	2610	1210	470PF	—	2.7 UF	—	2.7 UF

5. ALL DIODES ARE PEC PART NO 300-4446.
4. U1 IS PEC PART NO 700-7416.
3. ALL RESISTORS IN OHMS, 1/4 W, 5 %.
2. FOR ASSY SEE DRAWING NO. 102094. FOR SPECIFICATION SEE DRAWING NO. 101397.
[1] SEE VERSION TABLE FOR VALUES.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
.XX ± .010 ANGULAR ± 1/2°
.XXX ± .005
X ± 1/64
X ± 33
BREAK ALL SHARP CORNERS
APPROX .010

SIGNATURES	DATE
DR	9/23/71
CHK	9/23/71
DES	
ENGR	9/1/71
ENGR	

PEC PERIPHERAL EQUIPMENT CORPORATION

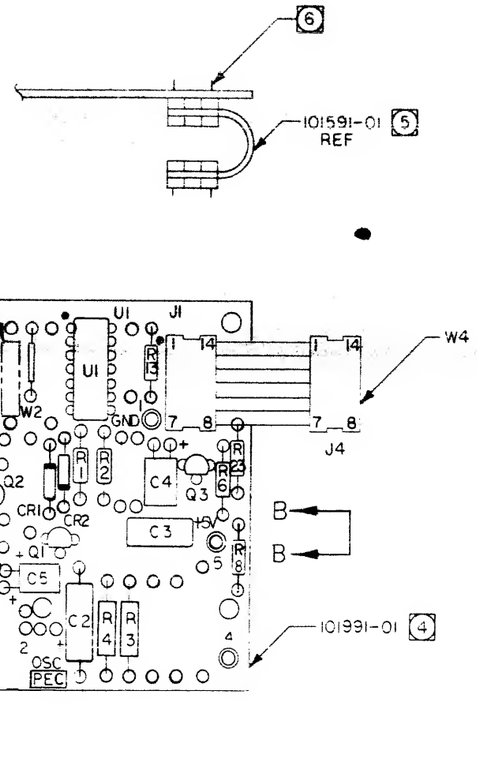
TITLE
SCHEMATIC - SINGLE TRACKING OSCILLATOR

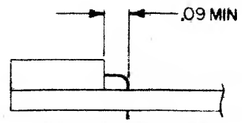
102094	1600
NEXT ASSY	1ST USED ON
APPLICATION	

FINISH:
MATL:

SIZE D | DWG NO. 102093 | REV A
SCALE NONE | DO NOT SCALE DWG | SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 385	3/8/71	[illegible]	[illegible]	[illegible]



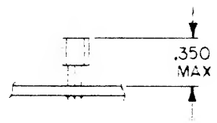


TYP C1,C4&C5

VIEW C-C

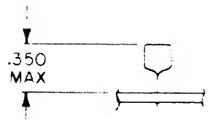
SCALE 4/1

R5 REMOVED FOR CLARITY



VIEW A-A

ROTATED 90° CCW



TYP C3

VIEW B-B

ROTATED 90° CW

7 TABLE I

PART NO.	REF. DES.
100-1025	R9,13,23
100-1535	R6
100-6815	R8
100-1515	R1
100-6805	R2
104-4220	R3
104-6810	R7
100-2225	R10
124-1020	R5
132-2752	C4
130-4715	C3
300-4446	CR1,2
200-4125	Q4
200-4123	Q1,2,3
700-7416	U1
100373-02	W2
101591-01	W4

8 TABLE II

DASH NO.	NRZ TAPE SPEEDS (IPS)	R4	R11	R12	C1	C2	C5
-01	31< 40	104-1331	104-1621	104-7500	132-2752	130-3315	132-2752
-02	24< 31	104-1471	104-2371	104-1101	132-2752	130-4715	132-2752
-03	14.5< 22	104-7500	104-8250	104-3830	132-2262	131-1020	——
-04	11< 14.5	104-8250	104-1211	104-5620	132-2262	31-1520	——
-05	7.5< 11	104-1001	104-1471	104-6810	132-2262	131-1520	——
-06	5< 7.5	104-1001	104-2371	104-1101	132-2262	131-2220	——
-07	40< 56	104-9090	104-1471	104-6810	132-2752	130-3315	132-2752
-08	56< 90	104-8250	104-8250	104-3630	132-2752	130-2215	132-2752
-09	22< 24	104-1781	104-2611	104-1211	132-2752	130-4715	132-2752

8. FOR PART NO.S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.
7. FOR PART NO.S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.
6. CLIP LEADS AFTER WAVE SOLDERING. ALL LEADS SHALL EXTEND A MAXIMUM OF .045 INCH THRU BOARD.
5. BEND CABLE APPROXIMATELY AS SHOWN BEFORE WAVE SOLDERING.
4. THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101991-01 REV "C" AND SUBSEQUENT.
3. RUBBER STAMP PART NO. INCLUDING VERSION NO. AND ISSUE LETTER.
2. ASSEMBLE PER STANDARD MFG METHODS.
1. REFERENCE DRAWINGS: SCHEMATIC-102093.
SPECIFICATION-101397.

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
XX ± .010
XXX ± .005
X ± 1/32
ANGULAR ± 1/2°
BREAK ALL SHARP CORNERS
APPROX .010

SIGNATURES		DATE
DR	[illegible]	2/24/71
CHK	[illegible]	2/24/71
DES		
ENGR	[illegible]	3/4/71
ENGR		

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE
PCBA-
SINGLE TRACKING
OSCILLATOR

TOP ASSY	1600
NEXT ASSY	1ST USED ON
APPLICATION	

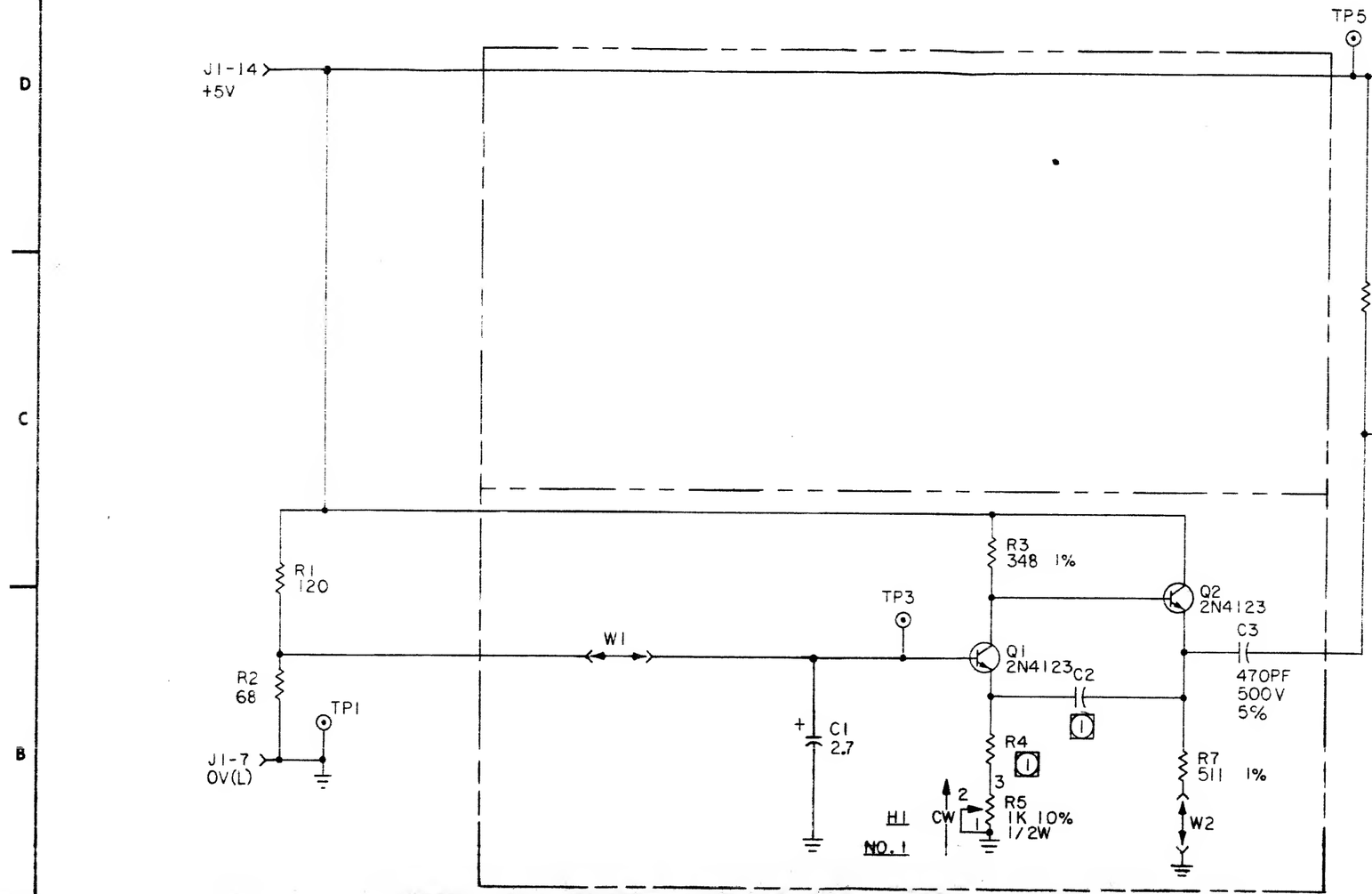
FINISH:

MATL:

SIZE D | CODE IDENT NO | DWG NO. 102094 | REV A

SCALE 2/1 | DO NOT SCALE DWG | SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 3-BW	18 FEB 1971			



VERSION TABLE (1)			
DASH NO.	TAPE SPEED (IPS)	R4, 1%	C2, 100V, 10%
-01	3.75<4.75/4.75<7	1330	.01
-02	4.75<7 / 7<9	619	.01
-03	7<9 / 9<13	1000	.0068
-04	9<13 / 13<18	1000	.0047
-05	13<18 / 18<26	1000	.0033
-06	18<26 / 26<33	1000	.0022
-07	26<33 / 33<42	1330	.0015
-08	33<42 / 42<55	1000	.0015
-09	42<55 / 55<85	1330	.001
-10	55<85 / 85<125	750	.001

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C4	
Q3	
R8	
W2	
TP5	TP2

5. ALL CAPACITOR VALUES ARE IN MICROFARADS, 35V, 20%.
4. ALL RESISTOR VALUES ARE IN OHMS, 1/4W 5%.
3. FOR ASSEMBLY DRAWING SEE 102096.
2. FOR SPECIFICATION SEE 101360.
(1) SEE VERSION TABLE FOR VALUE.
NOTES: UNLESS OTHERWISE SPECIFIED.

102096	1600
NEXT ASSY	1ST USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES
XX ± .010 ANGULAR ± 1/2°
XXX ± .005
X ± 1/32
BREAK ALL SHARP CORNERS APPROX. .010

SIGNATURES		DATE
DR		18 FEB 1971
CHK		2/19/71
DES		
ENGR		3/1/71
ENGR		

FINISH:
MATL:

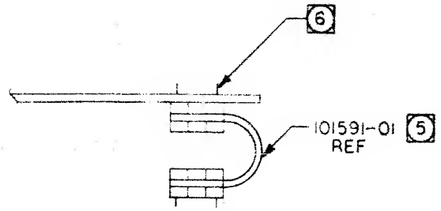
PEC PERIPHERAL EQUIPMENT CORPORATION

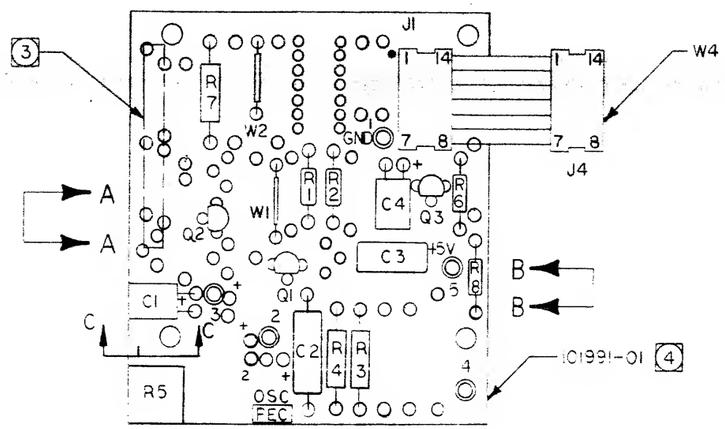
TITLE
SCHEMATIC — SINGLE FIXED OSCILLATOR

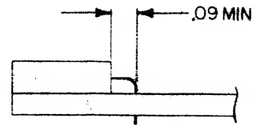
SIZE	DRAWING NO.	REV
D	102095	A

SCALE NONE DO NOT SCALE DWG SHEET 1 OF 1

REVISIONS					
REV	DESCRIPTION	DATE	DR	CHK	APPR
A	ERN 3-BW	3/9/71	DMR	JG	KG
B	ECN 2483	3/4/71	TB	JG	KG



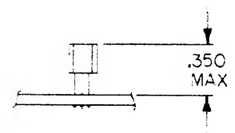




TYP C1,C4

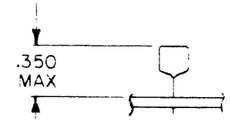
VIEW C-C

SCALE 4/1



VIEW A-A

ROTATED 90° CCW



VIEW B-B

ROTATED 90° CW

(7) TABLE I

PART NO.	REF. DES.
100-1535	R6
100-6815	R8
100-1215	R1
100-6805	R2
104-3480	R3
104-5110	R7
124-1020	R5
132-2752	C1,4
130-4715	C3
200-4123	Q1,2,3
100373-02	W1,2
101591-01	W4

(8) TABLE II

DASH NO.	TAPE SPEED (IPS) NRZ	TAPE SPEED (IPS) PE	R4	C2
-01	3.75<4.75	4.75<7	104-1331	131-1030
-02	4.75<7	7<9	104-6190	131-1030
-03	7<9	9<13	104-1001	131-6820
-04	9<13	13<18	104-1001	131-4720
-05	13<18	18<26	104-1001	131-3320
-06	18<26	26<33	104-1001	131-2220
-07	26<33	33<42	104-1331	131-1520
-08	33<42	42<55	104-1001	131-1520
-09	42<55	55<85	104-1331	131-1020
-10	55<85	85<125	104-7500	131-1020

(8) FOR PART NO.S WHICH ARE AFFECTED BY VERSION NO. SEE TABLE II.

(7) FOR PART NO.S WHICH ARE NOT AFFECTED BY VERSION NO. SEE TABLE I.

(6) CLIP LEADS AFTER WAVE SOLDERING. ALL LEADS SHALL EXTEND A MAXIMUM OF .045 INCH THRU BOARD.

(5) BEND CABLE APPROXIMATELY AS SHOWN BEFORE WAVE SOLDERING.

(4) THIS ASSY SHALL BE MADE FROM PROCESS BOARD 101991-01 REV "C" AND SUBSEQUENT.

(3) RUBBER STAMP PART NO. INCLUDING VERSION NO. AND ISSUE LETTER.

2. ASSEMBLE PER STANDARD MFG METHODS.

1. REFERENCE DRAWINGS: SCHEMATIC-102095.
SPECIFICATION-101360.

NOTES: UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES:
XX ± .010 ANGULAR ± 1/2°
XXX ± .005
X/X ± 1/33
BREAK ALL SHARP CORNERS
APPROX. .010

SIGNATURES		DATE
DR	L.S. Brown	3/9/71
CHK	Lee Johnson	3/4/71
DES		
ENGR	R. Johnson	3/4/71
ENGR		

FINISH:

MATL:

PEC PERIPHERAL EQUIPMENT CORPORATION

TITLE
PCBA-
SINGLE FIXED
OSCILLATOR

TOP ASSY	1600
NEXT ASSY	1ST USSB ON
APPLICATION	

SIZE	CODE IDENT. NO	DWG NO.	REV
D		102096	B

SCALE 2/1 DO NOT SCALE DWG SHEET 1 OF 1